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Evaluating the AD7292 10-Bit Monitor and Control System

FEATURES

- Full featured evaluation board for the AD7292
- Operates from a single 5 V power supply
- PC control in conjunction with the system demonstration platform (EVAL-SDP-CB1Z)
- PC software for control and data analysis (time and frequency domain)
- Standalone capability

ONLINE RESOURCES

- Evaluation Kit Contents
  - EVAL-AD7292SDZ evaluation board
  - Evaluation software CD for AD7292
  - USB cable
- Documents Needed
  - AD7292 data sheet
  - EVAL-AD7292SDZ user guide
- Required Software
  - EVAL-AD7292SDZ evaluation software
- Design and Integration Files
  - Schematics, layout files, bill of materials

EQUIPMENT NEEDED

- EVAL-AD7292SDZ evaluation board
- EVAL-SDP-CB1Z system demonstration platform
- Precision analog signal source
- SMB connectors/cables
- USB cable
- PC running Windows with USB 2.0 port

GENERAL DESCRIPTION

This user guide describes the evaluation board for the AD7292, which is a 10-bit monitor and control system integrated circuit with ADCs, DACs, a temperature sensor, and GPIOs. The AD7292 contains all the functions required for general-purpose monitoring of analog signals and control of external devices integrated into a single-chip solution. The AD7292 includes an 8-channel, 10-bit SAR ADC; four 10-bit DACs; a ±1°C accurate internal temperature sensor; and 12 GPIOs to aid system monitoring and control. Full details about the device are available in the AD7292 data sheet, which should be consulted in conjunction with this user guide when using the evaluation board.

On-board components of the evaluation board include the ADP170 low dropout, CMOS linear regulator and the AD8066 high speed, low noise amplifier. The evaluation board can be used in conjunction with the SDP demonstration platform or in standalone mode. The Link Configuration Options section of this user guide should be consulted when configuring the device for standalone operation.

PLEASE SEE THE LAST PAGE FOR AN IMPORTANT
WARNING AND LEGAL TERMS AND CONDITIONS.

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REVISION HISTORY

10/12—Revision 0: Initial Revision

FUNCTIONAL BLOCK DIAGRAM

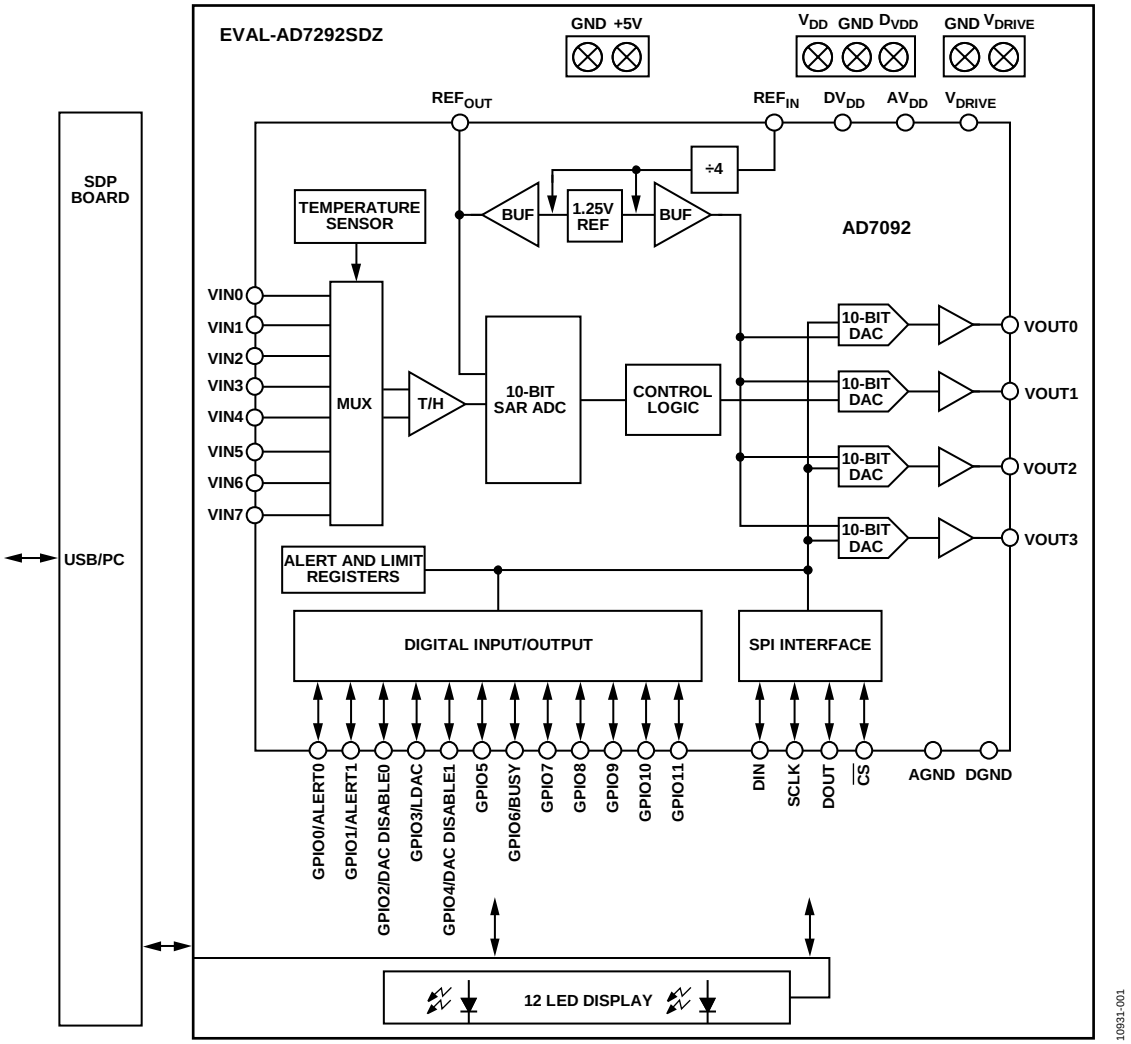

Figure 1.

GETTING STARTED

QUICK START STEPS

To begin using the evaluation board, do the following:

1. With the EVAL-SDP-CB1Z board disconnected from the USB port of the PC, install the AD7292 evaluation board software from the CD included in the evaluation board kit. The PC must be restarted after the software installation is complete. (For complete software installation instructions, see the Software Installation Procedures section.)
2. Connect the EVAL-SDP-CB1Z board to the EVAL-AD7292SDZ board as shown in Figure 2.
    a. Screw the two boards together using the nylon screw-nut set included in the evaluation board kit to ensure that the boards are connected firmly together.
3. Connect a 5 V dc power supply to Connecter J3 on the EVAL-AD7292SDZ board.
4. Connect the EVAL-SDP-CB1Z board to the PC using the supplied USB cable. If you are using Windows® XP, you may need to search for the EVAL-SDP-CB1Z drivers. Choose to automatically search for the drivers for the EVAL-SDP-CB1Z board if prompted by the operating system.
5. Launch the EVAL-AD7292SDZ software from the **Analog Devices** subfolder in the **Programs** menu.
6. If it is required to use the EVAL-AD7292SDZ board with an application specific development board, review the Modes of Operation section.

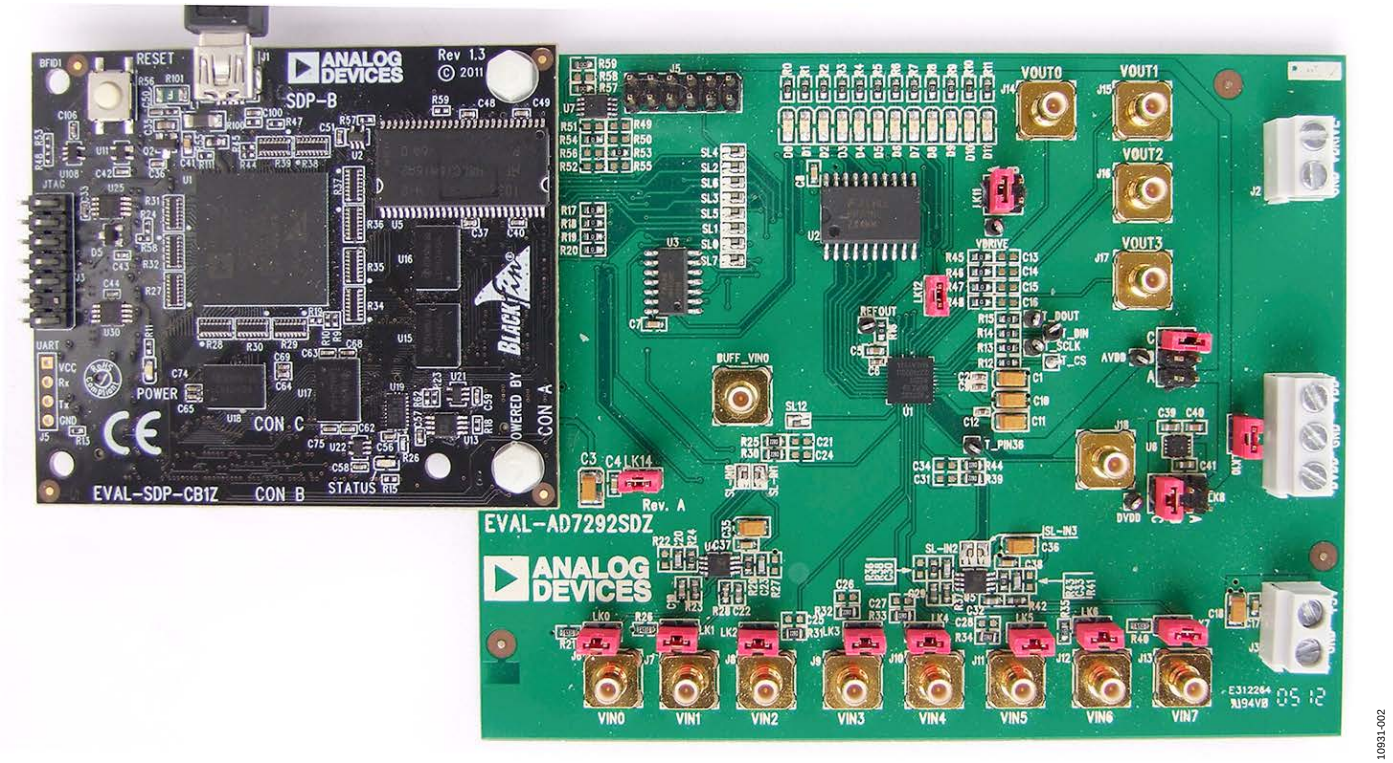

Figure 2. Hardware Configuration—Setting Up the EVAL-AD7292SDZ (EVAL-SDP-CB1Z on Left and EVAL-AD7292SDZ on Right)

SOFTWARE INSTALLATION PROCEDURES

The EVAL-AD7292SDZ evaluation kit includes a CD containing software to be installed on your PC before you begin using the evaluation board.

There are two parts to the installation:

- AD7292 evaluation board software installation
- EVAL-SDP-CB1Z system demonstration platform board drivers installation

Warning

The evaluation software and drivers must be installed before connecting the evaluation board and EVAL-SDP-CB1Z board to the USB port of the PC to ensure that the evaluation system is correctly recognized when it is connected to the PC.

Installing the AD7292 Evaluation Board Software

To install the AD7292 evaluation board software,

1. With the EVAL-SDP-CB1Z board disconnected from the USB port of the PC, insert the installation CD into the CD-ROM drive.
2. Double-click the **setup.exe** file to begin the evaluation board software installation. The software is installed to the following default location: **C:\Program Files\Analog Devices\AD7292**.
3. A dialog box appears asking for permission to allow the program to make changes to your computer. Click **Yes**.

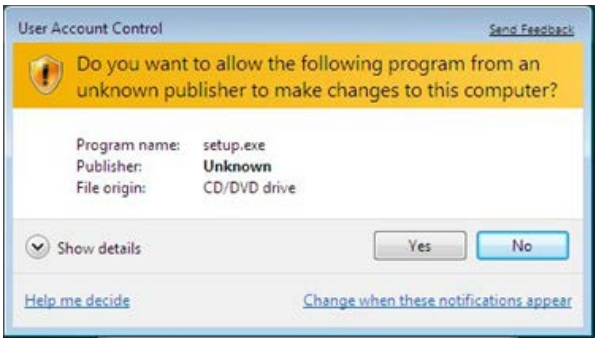

Figure 3. AD7292 Evaluation Software Installation: Granting Permission for Program to Make Changes

4. Select the location to install the software, and then click **Next**. (Figure 4 shows the default locations, which are displayed when the window opens, but you can select another location by clicking **Browse**.)

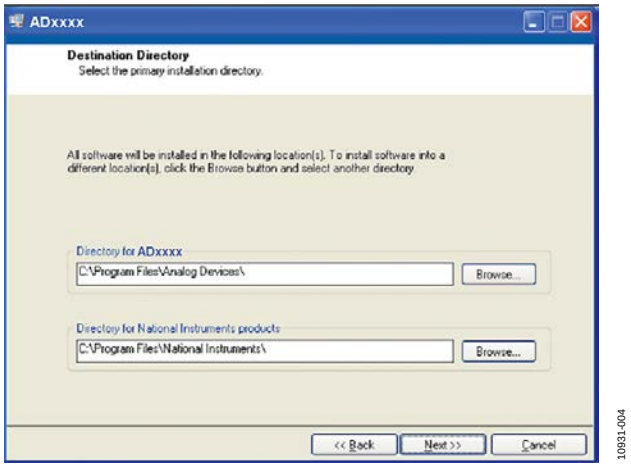

Figure 4. AD7292 Evaluation Software Installation: Selecting the Location for Software Installation

5. A license agreement appears. Read the agreement, and then select **I accept the License Agreement** and click **Next**.

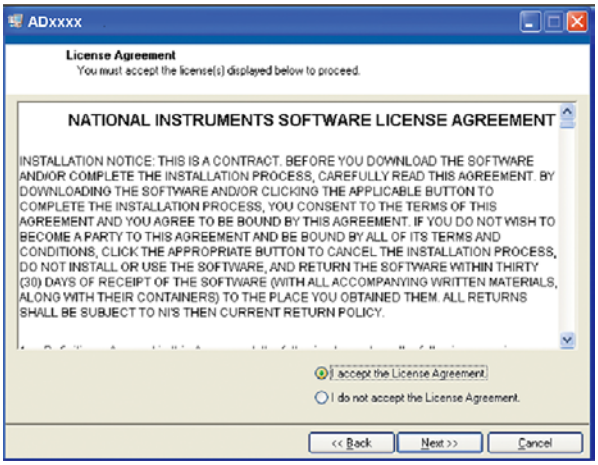

Figure 5. AD7292 Evaluation Software Installation: Accepting the License Agreement

6. A summary of the installation is displayed. Click **Next** to continue.

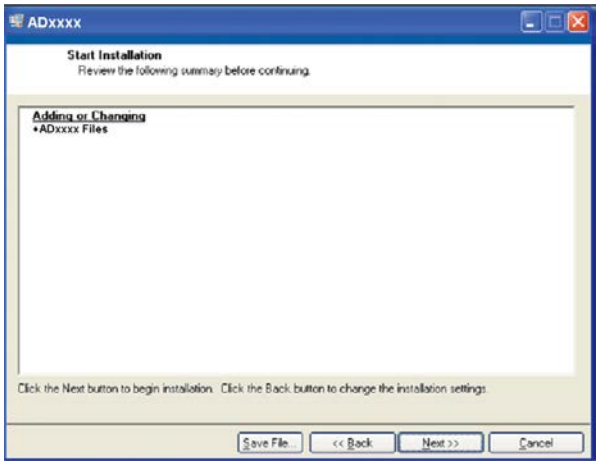

Figure 6. AD7292 Evaluation Software Installation: Reviewing a Summary of the Installation

7. A dialog box informs you when the installation is complete. Click **Next**.

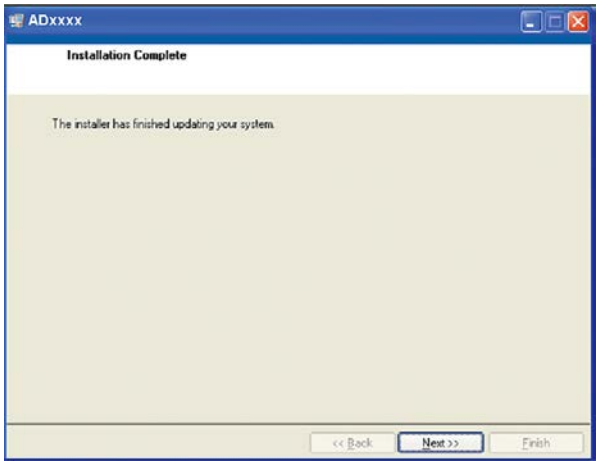

Figure 7. AD7292 Evaluation Software Installation: Indicating When the Installation is Complete

Installing the EVAL-SDP-CB1Z System Demonstration Platform Board Drivers

After the installation of the evaluation software is complete, a welcome window is displayed for the installation of the EVAL-SDP-CB1Z system demonstration platform board drivers.

1. With the EVAL-SDP-CB1Z board still disconnected from the USB port of the PC, make sure that all other applications are closed, and then click **Next**.

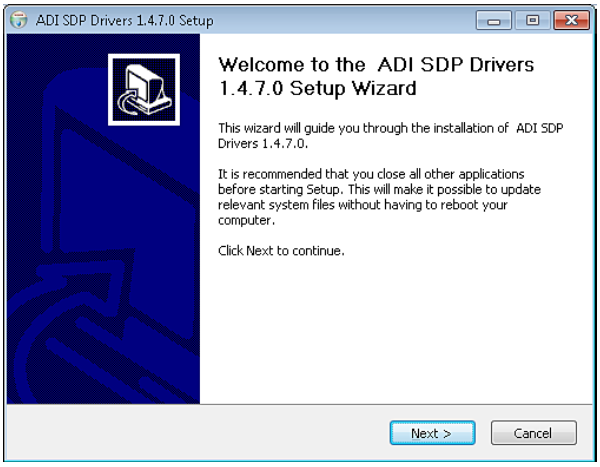

Figure 8. EVAL-SDP-CB1Z Drivers Setup: Beginning the Drivers Installation

2. Select the location to install the drivers, and then click **Next**.

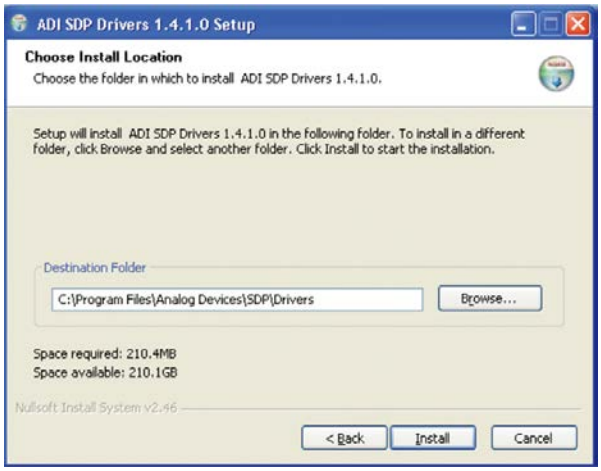

Figure 9. EVAL-SDP-CB1Z Drivers Setup: Selecting the Location for Drivers Installation

3. Click **Install** to confirm that you would like to install the drivers.

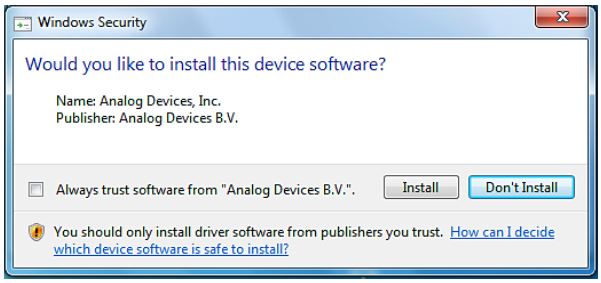

Figure 10. EVAL-SDP-CB1Z Drivers Setup: Granting Permission to Install Drivers

4. To complete the drivers installation, click **Finish**, which closes the installation wizard.

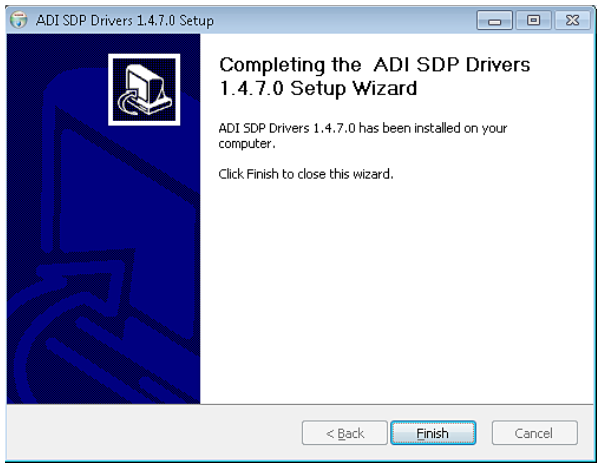

Figure 11. EVAL-SDP-CB1Z Drivers Setup: Completing the Drivers Setup Wizard

5. Before using the evaluation board, you must restart your computer.

EVALUATION BOARD SETUP PROCEDURES

After following the instructions in the Software Installation Procedures section, set up the evaluation and SDP boards as detailed in this section.

Warning

The evaluation software and drivers must be installed before connecting the evaluation board and EVAL-SDP-CB1Z board to the USB port of the PC to ensure that the evaluation system is correctly recognized when it is connected to the PC.

Configuring the Evaluation and SDP Boards

1. Connect the EVAL-SDP-CB1Z board to the EVAL-AD7292SDZ board as shown in Figure 2.
   a. Screw the two boards together using the nylon screw-nut set included in the evaluation board kit to ensure that the boards are connected firmly together.
2. Connect a 5 V dc power supply to Connecter J3 of the EVAL-AD7292SDZ board.
3. Connect the EVAL-SDP-CB1Z board to the PC using the supplied USB cable.
4. If it is required to use the EVAL-AD7292SDZ board with an application specific development board, review the Modes of Operation section.

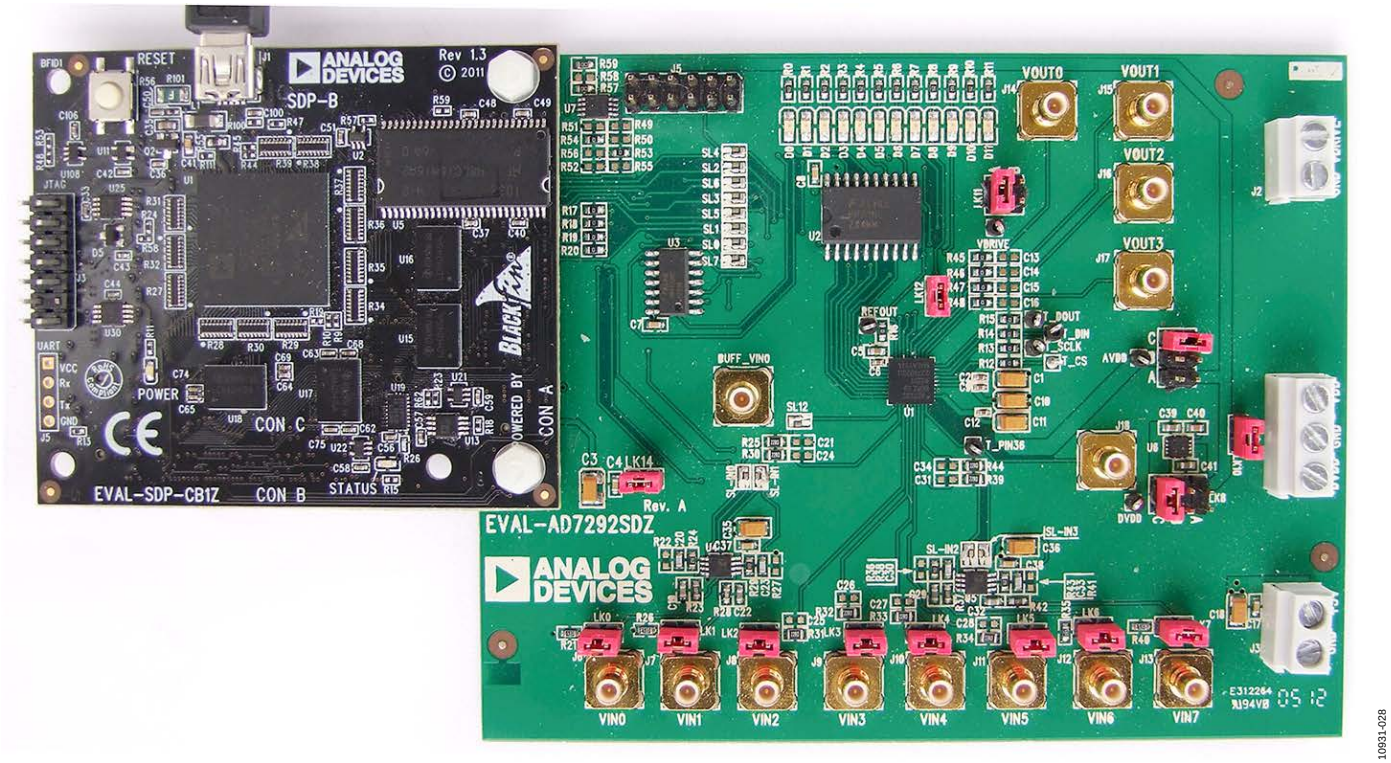

Figure 12. Hardware Configuration—Setting Up the EVAL-AD7292SDZ (EVAL-SDP-CB1Z on Left and EVAL-AD7292SDZ on Right)

EVALUATION BOARD HARDWARE

POWER SUPPLIES

When the EVAL-AD7292SDZ board is used in conjunction with the EVAL-SDP-CB1Z board (serial interface mode), the V_{DRIVE} supply is provided from the SDP board. A 5 V supply should be applied to J3. Each supply is decoupled on the EVAL-AD7292SDZ board. A single ground plane is used on this board to minimize the effect of high frequency noise interference.

INPUT SIGNALS

There are eight input channels, VIN0 to VIN7, where an input signal between 0 V and 5 V can be applied. Refer to the schematic diagram that is available on the EVAL-AD7292SDZ Web page. VIN2 to VIN5 are directly connected to the AD7292 device inputs via a 22 Ω resistor, and provision for a low-pass filter capacitor is available on the PCB. The links on each of these inputs hold the input to GND and should be removed when using any of the inputs V_{IN2} to V_{IN5}.

The other inputs—VIN0, VIN1, VIN6, and VIN7—are buffered through a AD8066 device in a noninverting configuration. The links on each of these inputs hold the input to GND via a 50 Ω resistor.

OUTPUT SIGNALS

There are four output channels, V_{OUT0} to V_{OUT3}, where an output signal between 0 V and 5 V can be generated by the internal DACs. The outputs are directly connected to the AD7292 device outputs via a 0 Ω resistor, and provision for a low-pass filter capacitor is available on the PCB. Refer to the schematic diagram that is available on the EVAL-AD7292SDZ Web page.

LINK CONFIGURATION OPTIONS

There are multiple link (LKn) and solder link (SLn) options that must be set correctly to select the appropriate operating setup before you begin using the evaluation board. The functions of these options are outlined in Table 1.

Setup Conditions

Care should be taken before applying power and signals to the evaluation board to ensure that all link positions are as required by the operating mode. There are two modes in which to operate the evaluation board. The evaluation board can be operated in serial interface mode to be used with the SDP board, or the evaluation board can be used in standalone mode.

Table 2 shows the position in which all the links are set when the evaluation board is packaged. When the board is shipped, it is assumed that the user is operating with the SDP board. The links are set so that the control signals and V_{DRIVE} are supplied by the SDP board. An external 5 V dc power supply must be applied to External Connector J3.

Table 1. Link Option Functions

Link	Function
LK0	When inserted, this link connects the VIN0 input to a 50 Ω input resistor tied to ground. The input is floating when this link is not inserted.
LK1	When inserted, this link connects the VIN1 input to a 50 Ω input resistor tied to ground. The input is floating when this link is not inserted.
LK2	When inserted, this link connects the VIN2 input to ground. The input is floating when this link is not inserted.
LK3	When inserted, this link connects the VIN3 input to ground. The input is floating when this link is not inserted.
LK4	When inserted, this link connects the VIN4 input to ground. The input is floating when this link is not inserted.
LK5	When inserted, this link connects the VIN5 input to ground. The input is floating when this link is not inserted.
LK6	When inserted, this link connects the VIN6 input to a 50 Ω input resistor tied to ground. The input is floating when this link is not inserted.
LK7	When inserted, this link connects the VIN7 input to a 50 Ω input resistor tied to ground. The input is floating when this link is not inserted.
LK8	This link option determines the voltage applied to the DVDD pin of the AD7292. In Position A, the internal 3.3 V supply is applied to the DVDD pin. In Position B, the voltage applied to Jumper J4-1 is applied to the DVDD pin. In Position C, the 5 V supply is applied to the DVDD pin if the 5 V supply is connected to the J3 connector.
LK9	This link option determines the voltage applied to the AVDD pin of the AD7292. In Position A, the internal 3.3 V supply is applied to the AVDD pin. In Position B, the voltage applied to Jumper J4-3 is applied to the AVDD pin. In Position C, the 5 V supply is applied to the AVDD pin if the 5 V supply is connected to the J3 connector.
LK10	When this link is inserted, Jumper Connections J4-1 (which is connected to DVDD) and J4-3 (which is connected to AVDD) are tied together.
LK11	In Position A, the V_{DRIVE} voltage is supplied by the SDP VIO_CONNECTOR from the SDP board. In Position B, the V_{DRIVE} voltage must be supplied via External Connector J2.
LK12	When inserted, this link connects Pin 14 of the AD7292 to ground.
LK14	When inserted, this link connects the 5 V supply to Pin 1 of the SDP connector (J1).
SL-IN0	This solder link option determines whether an input amplifier is used on the VIN0 analog input channel. In Position A, there is no amplifier included in the analog input channel path. In Position B, there is an amplifier included in the analog input channel path.
SL-IN1	This solder link option determines whether an input amplifier is used on the VIN1 analog input channel. In Position A, there is no amplifier included in the analog input channel path. In Position B, there is an amplifier included in the analog input channel path.
SL-IN2	This solder link option determines whether an input amplifier is used on the VIN6 analog input channel. In Position A, there is no amplifier included in the analog input channel path. In Position B, there is an amplifier included in the analog input channel path.
SL-IN3	This solder link option determines whether an input amplifier is used on the VIN7 analog input channel. In Position A, there is no amplifier included in the analog input channel path. In Position B, there is an amplifier included in the analog input channel path.
SL0	This solder link option determines whether the GPIO0 pin is routed to the GPIO0 connector of the SDP board or to Connector J5-1. In Position A, the pin is routed to the GPIO0 connector of the SDP. In Position B, the pin is routed to Connector J5-1.
SL1	This solder link option determines whether the GPIO1 pin is routed to the GPIO1 connector of the SDP board or to Connector J5-2. In Position A, the pin is routed to the GPIO1 connector of the SDP. In Position B, the pin is routed to Connector J5-2.
SL2	This solder link option determines whether the GPIO2 pin is routed to the GPIO2 connector of the SDP board or to Connector J5-3. In Position A, the pin is routed to the GPIO2 connector of the SDP. In Position B, the pin is routed to Connector J5-3.
SL3	This solder link option determines whether the GPIO3 pin is routed to the GPIO3 connector of the SDP board or to Connector J5-4. In Position A, the pin is routed to the GPIO3 connector of the SDP. In Position B, the pin is routed to Connector J5-4.

Link	Function
SL4	This solder link option determines whether the GPIO4 pin is routed to the GPIO4 connector of the SDP board or to Connector J5-5. In Position A, the pin is routed to the GPIO4 connector of the SDP. In Position B, the pin is routed to Connector J5-5.
SL5	This solder link option determines whether the GPIO5 pin is routed to the GPIO5 connector of the SDP board or to Connector J5-6. In Position A, the pin is routed to the GPIO5 connector of the SDP. In Position B, the pin is routed to Connector J5-6.
SL6	This solder link option determines whether the GPIO6 pin is routed to the GPIO6 connector of the SDP board or to Connector J5-7. In Position A, the pin is routed to the GPIO6 connector of the SDP. In Position B, the pin is routed to Connector J5-7.
SL7	This solder link option determines whether the GPIO7 pin is routed to the GPIO7 connector of the SDP board or to Connector J5-8. In Position A, the pin is routed to the GPIO7 connector of the SDP. In Position B, the pin is routed to Connector J5-8.
SL12	This solder link option determines whether the voltage from SL-IN0 is routed to the VIN0 SMB connector or to the BUFF_VIN0 SMB connector. In Position A, the input is routed to SMB Connector VIN0. In Position B, the input is routed to SMB Connector BUFF_VIN0.

Table 2. Default Link Positions for Packaged EVAL-AD7292SDZ

Link No.	Position	Function
LK0	Inserted	Connects the VIN0 input to a 50 Ω input resistor tied to ground.
LK1	Inserted	Connects the VIN1 input to a 50 Ω input resistor tied to ground.
LK2	Inserted	Connects the VIN2 input to ground.
LK3	Inserted	Connects the VIN3 input to ground.
LK4	Inserted	Connects the VIN4 input to ground.
LK5	Inserted	Connects the VIN5 input to ground.
LK6	Inserted	Connects the VIN6 input to a 50 Ω input resistor tied to ground.
LK7	Inserted	Connects the VIN7 input to a 50 Ω input resistor tied to ground.
LK8	Position C	Connects DVDD to 5 V.
LK9	Position C	Connects AVDD to 5 V.
LK10	Inserted	Connects DVDD and AVDD together (via J4-1 and J4-3).
LK11	Position A	V_{DRIVE} voltage is supplied by the SDP board VIO_CONNECTOR.
LK12	Inserted	Connects Pin 14 of the AD7292 to ground.
LK14	Inserted	Connects the 5 V supply to Pin 1 of J1 to supply power to the SDP board.
SL-IN0	Position B	Amplifier U4-A is included on the analog input channel path from SMB Connector VIN0.
SL-IN1	Position B	Amplifier U4-B is included on the analog input channel path from SMB Connector VIN1.
SL-IN2	Position B	Amplifier U5-A is included on the analog input channel path from SMB Connector VIN6.
SL-IN3	Position B	Amplifier U5-B is included on the analog input channel path from SMB Connector VIN7.
SL0	Position A	Signal to/from GPIO0 pin is routed to GPIO0 connector of the SDP.
SL1	Position A	Signal to/from GPIO1 pin is routed to GPIO1 connector of the SDP.
SL2	Position A	Signal to/from GPIO2 pin is routed to GPIO2 connector of the SDP.
SL3	Position A	Signal to/from GPIO3 pin is routed to GPIO3 connector of the SDP.
SL4	Position A	Signal to/from GPIO4 pin is routed to GPIO4 connector of the SDP.
SL5	Position A	Signal to/from GPIO5 pin is routed to GPIO5 connector of the SDP.
SL6	Position A	Signal to/from GPIO6 pin is routed to GPIO6 connector of the SDP.
SL7	Position A	Signal to/from GPIO7 pin is routed to GPIO7 connector of the SDP.
SL12	Position B	Signal from SL-IN0 is routed to the BUFF_VIN0 SMB connector.

EVALUATION BOARD CIRCUITRY

OVERVIEW

The circuitry contained within the EVAL-AD7292SDZ board is designed to operate from a single 5 V power supply. It is also possible to connect an application specific power supply voltage to Connector J4 or to use the internal 3.3 V regulator based on the ADP170 device.

There are eight input channels, VIN0 to VIN7, where an input signal between 0 V and 5 V can be applied. VIN2 to VIN5 are directly connected to the AD7292 device inputs via a 22 Ω resistor, and provision for a low-pass filter capacitor is available on the PCB. The links on each of these inputs hold the input to GND and should be removed when using any of the following inputs: VIN2 to VIN5. The other inputs—VIN0, VIN1, VIN6, and VIN7—are buffered through a AD8066 device in a noninverting configuration. The links on each of these inputs hold the input to GND via a 50 Ω resistor.

The internal 1.25 V voltage reference of the AD7292 is used and allows a programmable voltage input range from 0 V to 1.25 V, 2.5 V, or 5 V and can be programmed for each input channel individually.

There are four output channels, VOUT0 to VOUT3, where an output signal between 0 V and 5 V can be generated by the internal DACs. The outputs are directly connected to the AD7292 device outputs via a 0 Ω resistor, and provision for a low-pass filter capacitor is available on the PCB.

The GPIO pins of the AD7292 are connected to a bank of LEDs and are also made available to PCB Header J5 via the SL0 to SL7 solder links.

SOCKETS AND CONNECTORS

There are 13 SMB input sockets and five tab connectors that affect the operation of the AD7292 on this evaluation board. When operating the board with the SDP board, an external 5 V supply is required for the AD7292 board. The functions of the SMB sockets are outlined in Table 3.

Table 3. Socket Functions

Socket	Function
VIN0 to VIN7	SMB socket for a single-ended input that is applied to the VIN0 to VIN7 pins of the AD7292.
VOUT0 to VOUT4	SMB socket for a single-ended output that comes from the VOUT1 to VOUT4 pins of the AD7292.
BUFF_VIN0	SMB socket for the buffered VIN0 input. (SL-IN0 and SL12 must be in Position B.)
J1	This connector connects the AD7292 board to the SDP board.
J2	In standalone mode, V_{DRIVE} should be supplied via this connector. (LK11 must be in Position B.)
J3	Connect a 5 V supply to this input.
J4	This connection provides the user with the option of connecting external voltages for the DVDD and AVDD pins. (If different voltages are required at these pins, ensure that LK10 is removed.)
J5	This 14-pin header connects to the GPIO pins of the AD7292.

MODES OF OPERATION

SERIAL INTERFACE MODE

The AD7292 uses a high speed serial interface that allows sampling rates of up to 1 MSPS. For more information about the operation of the serial bus, refer to the AD7292 data sheet.

The EVAL-AD7292SDZ communicates with the EVAL-SDP-CB1Z board using level shifters. The EVAL-SDP-CB1Z operates at a 3.3 V logic level, which allows V_{DRIVE} voltages that exceed 3.3 V to be used without damaging the SDP interface.

Details about the serial interface can be found in the AD7292 data sheet.

SDP Limitations

Due to software limitations of the EVAL-SDP-CB1Z, high sample rates entered into the dialog box may not reflect the actual sample rate running on the AD7292. In this case, the analysis results will not show true values. This may occur if the value for SCLK is too slow for a given sample rate entered.

This limitation does not apply when using the EVAL-AD7292SDZ in standalone mode.

STANDALONE MODE

The EVAL-AD7292SDZ can also be used without the EVAL-SDP-CB1Z controller board. In this case, the customer application board is connected to the digital interface using the J5 header connector (or, if preferred, using the test points), an external V_{DRIVE} voltage (ranging from 1.8 V to 5.25 V) is connected to J2, and LK11 is moved to Position B. Refer to the schematic diagram that is available on the EVAL-AD7292SDZ Web page for more details.

HOW TO USE THE SOFTWARE FOR EVALUATING THE AD7292

SETTING UP THE SYSTEM FOR DATA CAPTURE

After completing the steps in the Software Installation Procedures and Evaluation Board Setup Procedures sections, set up the system for data capture as follows:

1. Allow the **Found New Hardware Wizard** to run after the EVAL-SDP-CB1Z board is plugged into your PC. (If you are using Windows XP, you may need to search for the EVAL-SDP-CB1Z drivers. Choose to automatically search for the drivers for the EVAL-SDP-CB1Z board if prompted by the operating system.)
2. Check that the board is connecting to the PC correctly using the **Device Manager** of the PC.
   a. Access the **Device Manager** as follows:
      i. Right-click **My Computer** and then click **Manage**.
      ii. A dialog box appears asking for permission to allow the program to make changes to your computer. Click **Yes**.
      iii. The **Computer Management** box appears. Click **Device Manager** from the list of **System Tools** (see Figure 13).
   b. The EVAL-SDP-CB1Z board should appear under **ADI Development Tools**. This indicates that the driver software is installed and that the board is connecting to the PC correctly.

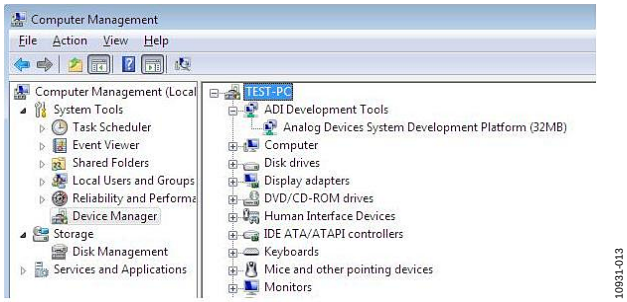

Figure 13. Device Manager: Checking that the Board Is Connected to the PC Correctly

Launching the Software

After completing the steps in the Setting Up the System for Data Capture section, launch the AD7292 software as follows:

1. From the **Start** menu, select **Programs** > **Analog Devices** > **AD7292.** The main window of the software then displays.
2. If the AD7292 evaluation system is not connected to the USB port via the EVAL-SDP-CB1Z when the software is launched, a connectivity error displays (see Figure 14). Connect the evaluation board to the USB port of the PC, wait a few seconds, click **Rescan**, and then follow the on-screen instructions.

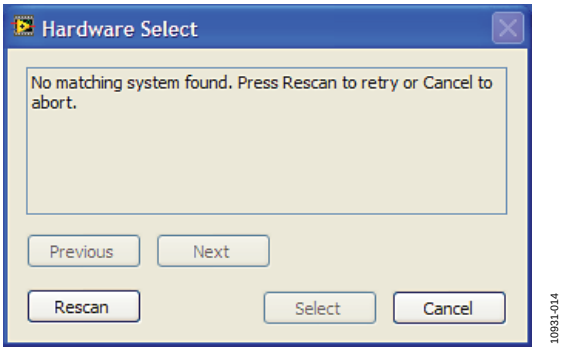

Figure 14. Connectivity Error Alert

When the software starts running, it searches for hardware connected to the PC. A dialog box indicates when the generic SDP attached to the PC is detected, and then the main window appears (see Figure 15).

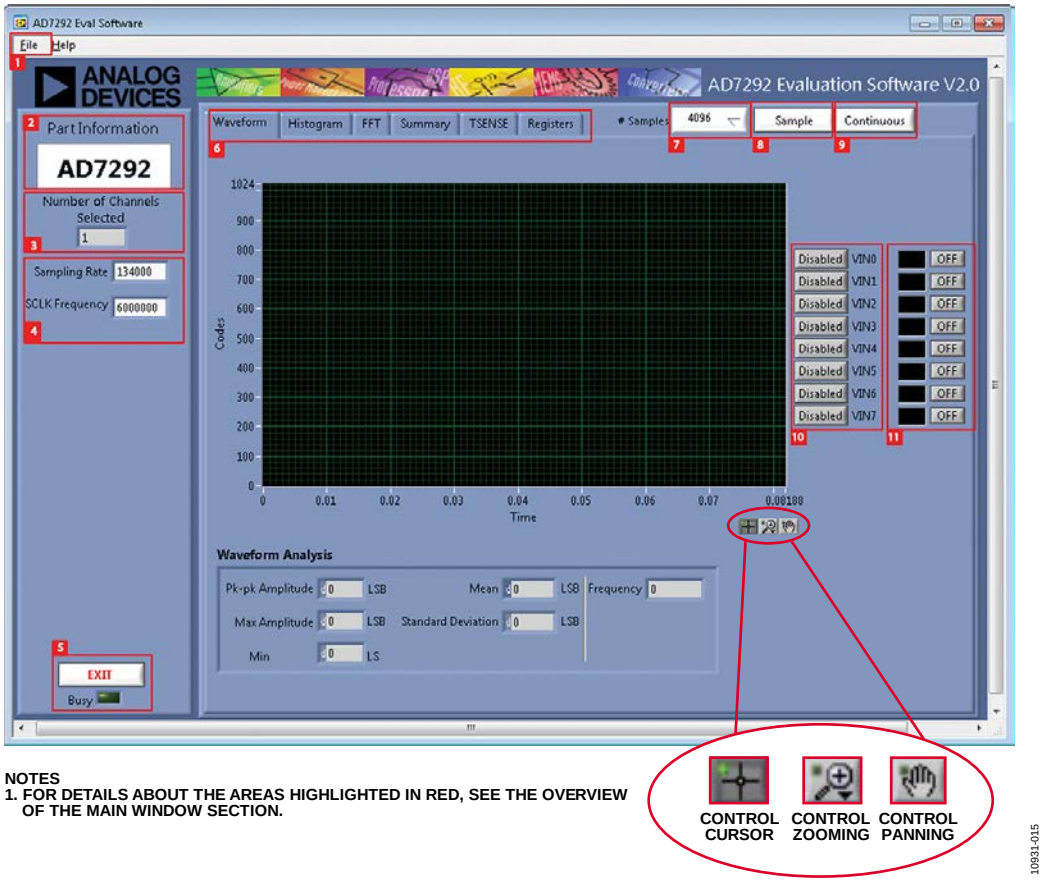

Figure 15. Evaluation Software Main Window: Setup Screen

OVERVIEW OF THE MAIN WINDOW

The main window of the software is shown in Figure 15 and has the features described in this section.

File Menu (Section 1)

The **File** menu (labeled 1 in Figure 15) offers the choice to

- **Load data**: load previously captured data or example files in .tsv (tab separated values) format for analysis (see Figure 16). (The default location for the example files is **C:\Program Files\Analog Devices\AD7292\examples**.)
- **Save Data as .tsv**: save captured data in .tsv format for future analysis (see Figure 17).
- **Print Front Panel Picture**: print the main window to your default printer.
- **Save Picture**: save the current screen capture.
- **Exit**: quit the application.

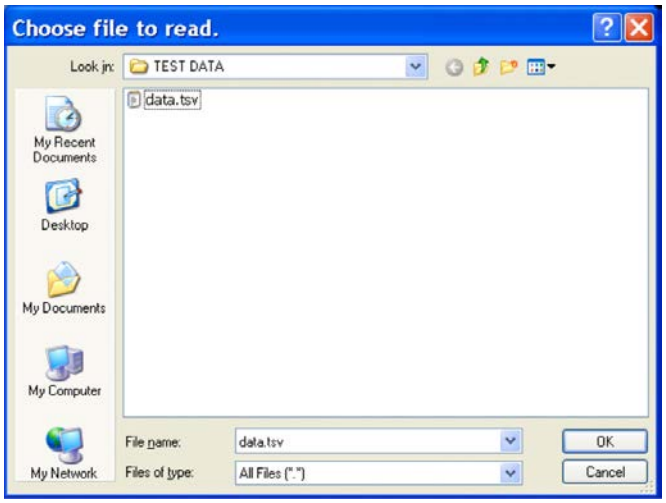

Figure 16. Load File Dialog Box:
Loading Previously Captured Data or Example Files in .tsv Format

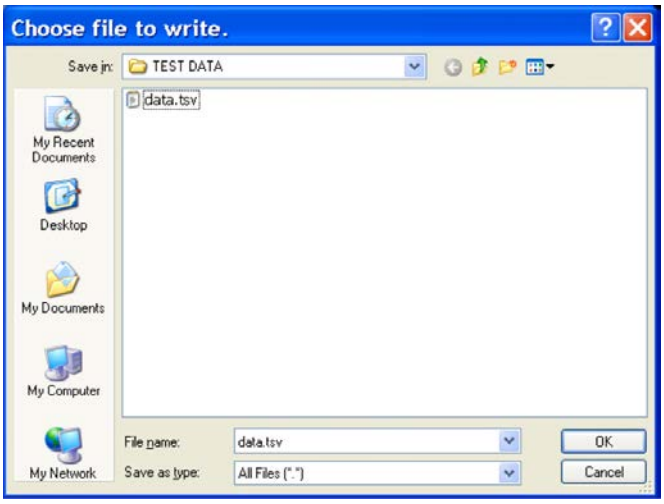

Figure 17. Save File Dialog Box: Saving Data as .tsv

Part Information Box (Section 2)

The **Part Information** box (labeled 2 in Figure 15) displays the generic being evaluated and is for informational purposes only.

Number of Channels Selected Box (Section 3)

The **Number of Channels Selected** box (labeled 3 in Figure 15) shows the total number of input channels that are enabled.

Sampling Rate and SCLK Frequency Boxes (Section 4)

The values entered into the **Sampling Rate** and **SCLK Frequency** boxes (labeled 4 in Figure 15) affect one another. The default sampling frequency matches the maximum sample rate of the ADC selected from the drop-down menu. Although you can adjust the sampling frequency, there are limitations in terms of the sample frequencies that can be entered. If an unusable sample frequencies is input, the software automatically adjusts the sample frequency accordingly. Units can be entered as, for example, 10k for 10,000 Hz. Because the maximum sample frequency is device dependent—some of the ADCs are capable of operating at up to 250 ksps while others can run to 1.3 MSPS—the software automatically adjusts the sample frequency according to the ability of the ADC being evaluated. For example, if you enter a value that is beyond the ability of the device, the software indicates this and reverts to the maximum sample frequency.

Exit Button (Section 5)

Clicking **Exit** (labeled 5 in Figure 15) closes the software. Alternatively, you can select **Exit** from the **File** menu.

Tabs Area (Section 6)

There are six tabs available in the tabs area (labeled 6 in Figure 15) of the main window: **Waveform**, **Histogram**, **FFT**, **Summary**, **TSENSE**, and **Registers**. These tabs display ADC data in different formats, and the Registers tab allows you to change the register configuration settings. Navigation tools are provided within each tab, with the exception of the **Registers** tab, to allow you to control the cursor, zooming, and panning (see Figure 15).

Each tab is described in more detail in the Generating a Waveform Analysis Report; Generating a Histogram of the ADC Code Distribution; Generating a Fast Fourier Transform of AC Characteristics; Generating a Summary of the Waveform, Histogram, and Fast Fourier Transform; Displaying Temperature Measurements; and Modifying Control Register Settings sections.

Samples Box (Section 7)

The **# Samples** box (labeled 7 in Figure 15) allows you to select the number of samples to analyze.

Sample Button (Section 8)

Clicking **Sample** (labeled 8 in Figure 15) performs a single capture.

Continuous Button (Section 9)

Clicking **Continuous** (labeled 9 in Figure 15) performs a continuous capture from the ADC. Clicking **Continuous** a second time stops sampling.

Enable ADC Input Channels Buttons (Section 10)

Clicking the buttons in this area (labeled 10 in Figure 15) enable or disable the respective ADC input channels.

Channel Display Buttons (Section 11)

Clicking the buttons in this area (labeled 11 in Figure 15) allows you to display multiple channel reads. (Note that for FFT analysis, you can select only one channel to be displayed.)

EVALUATION

EVALUATION PROCEDURES FOR EVAL-AD7292SDZ

Generating a Waveform Analysis Report

Figure 18 illustrates the waveform capture tab for a 5 V p-p, 1 kHz sine wave input signal.

The **Waveform Analysis** area reports the amplitudes recorded from the captured signal.

To scale the x-axis of the waveform diagram, right-click on the rightmost value and clear the autoscale function from the menu that appears. Then enter the required value.

To scale the y-axis of the waveform diagram, right-click on the topmost value and clear the autoscale function from the menu that appears. Then enter the required value.

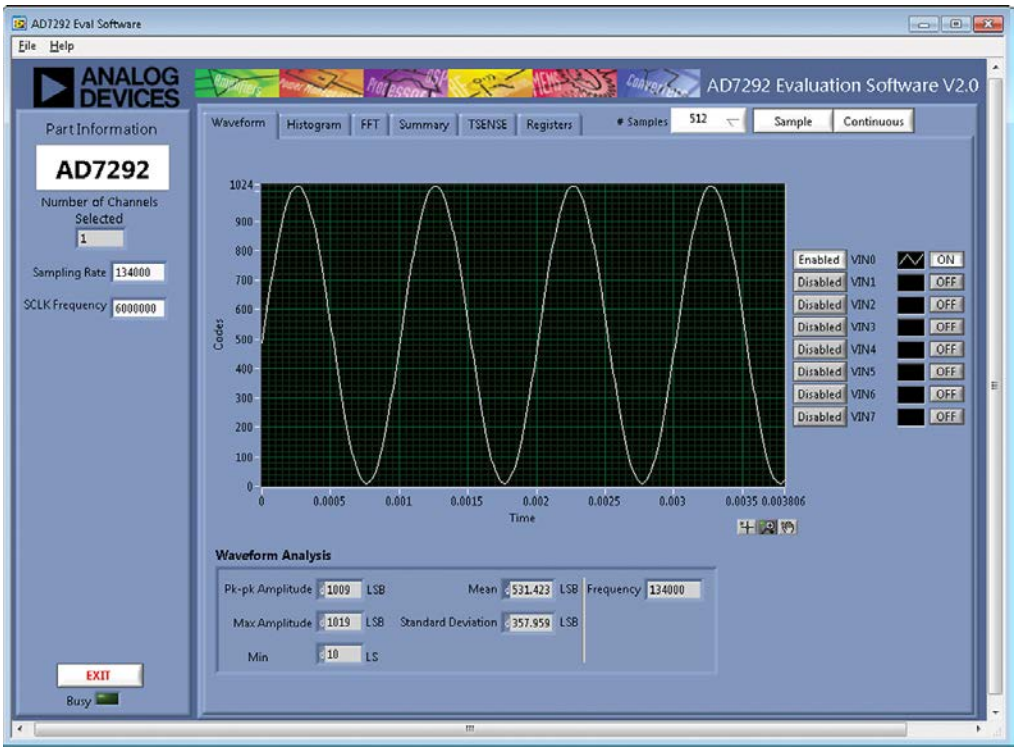

Figure 18. Waveform Tab

Generating a Histogram of the ADC Code Distribution

The **Histogram** tab can be used to perform ac testing or, more commonly, dc testing. This tab shows the ADC code distribution of the input and computes the mean and standard deviation, which are displayed as **Mean** and **Transition Noise**, respectively, in the **Histogram Analysis** area (see Figure 19).

Figure 19 shows the histogram for a 5 V p-p, 1 kHz sine wave applied to the ADC input and the resulting calculations.

AC Input

To perform a histogram test of ac input,

1. Apply a signal source to the VIN0 to VIN7 input connectors.
2. Click the **Histogram** tab from the main window.
3. Click **Sample**.

Raw data is then captured and passed to the PC for statistical computations, and various measured values are displayed in the **Histogram Analysis** area.

DC Input

To perform a histogram test of dc input,

1. If an external source is being used, apply a signal source.
2. Click the **Histogram** tab from the main window.
3. Click **Sample**.

Raw data is then captured and passed to the PC for statistical computations, and various measured values are displayed in the **Histogram Analysis** area.

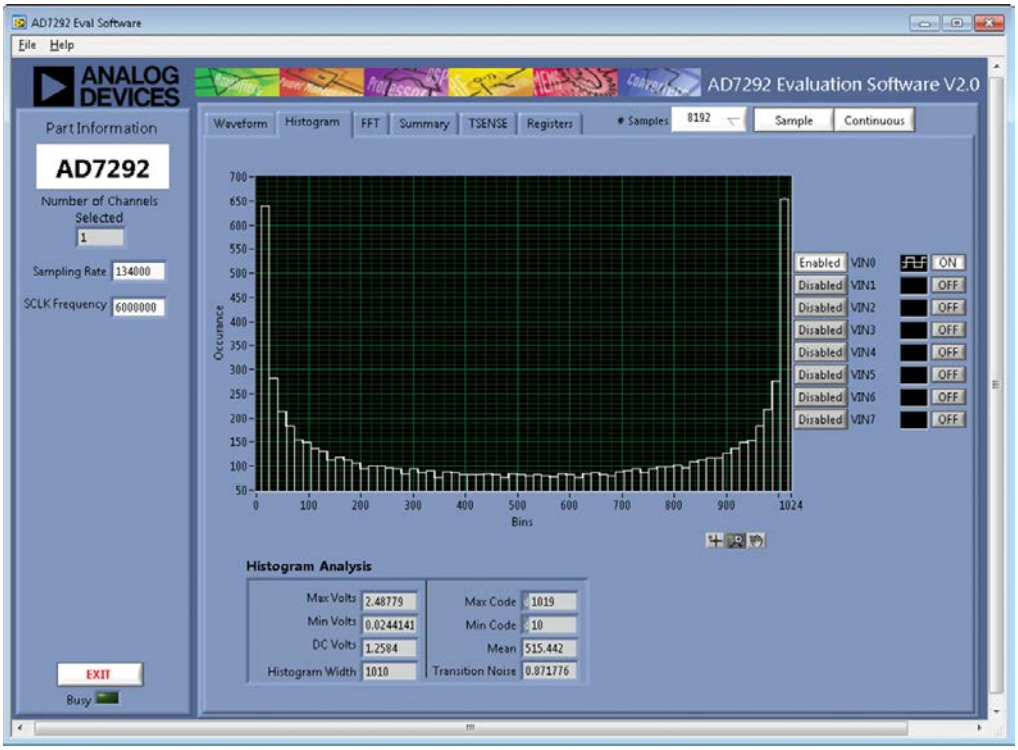

Figure 19. Histogram Tab

Generating a Fast Fourier Transform of AC Characteristics

Figure 20 shows the **FFT** tab. This feature tests the traditional ac characteristics of the converter and displays a fast Fourier transform (FFT) of the results.

To perform an ac FFT test,

1. Apply a sinusoidal signal with low distortion (better than 115 dB) to the evaluation board. To attain the requisite low distortion, which is necessary to allow true evaluation of the part, one option is to
   a. Filter the input signal from the ac source. Choose an appropriate band-pass filter based on the sinusoidal signal applied.
   b. If a low frequency band-pass filter is used when the full-scale input range is more than a few volts peak-to-peak, use the on-board amplifiers to amplify the signal, thus preventing the filter from distorting the input signal.
2. Click the **FFT** tab from the main window.
3. Click **Sample**.

As in the histogram test, raw data is then captured and passed to the PC, which performs the FFT and displays the resulting SNR, THD, and SINAD.

The **Spectrum Analysis** box displays the results of the captured data.

- The area labeled 1 in Figure 20 shows the input signal information.
- The area labeled 2 in Figure 20 displays the fundamental frequency and amplitude in addition to the second to fifth harmonics.
- The area labeled 3 in Figure 20 displays the performance data, including the SNR, THD, and SINAD.

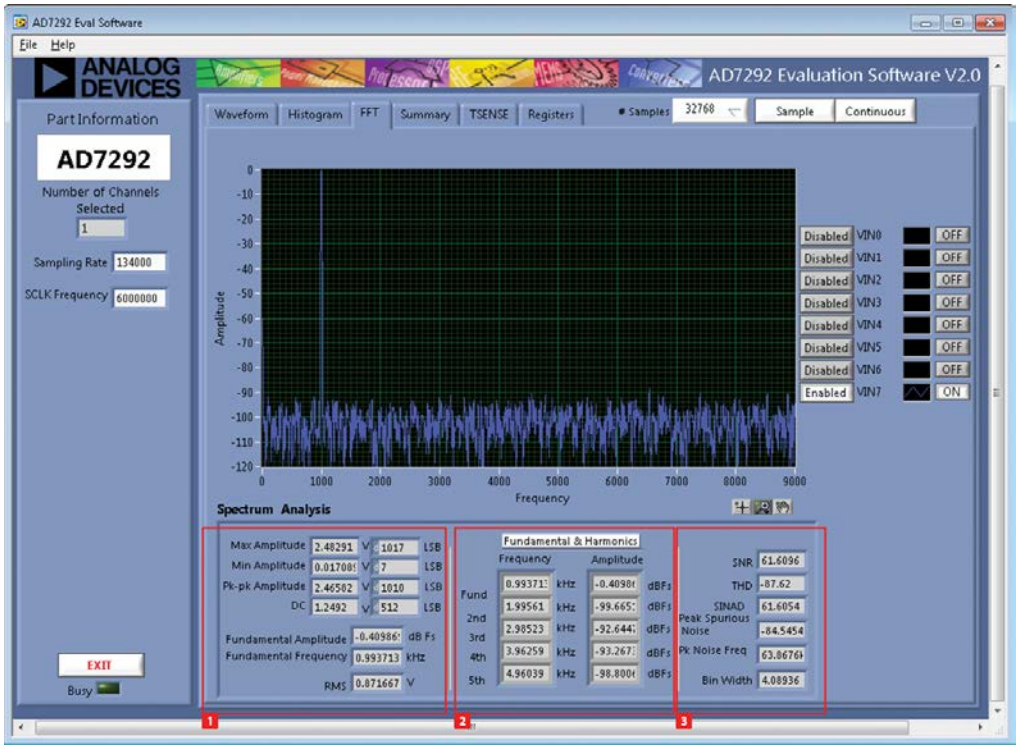

Figure 20. FFT Tab

Generating a Summary of the Waveform, Histogram, and Fast Fourier Transform

Figure 21 shows the **Summary** tab. The **Summary** tab captures all the display information and provides it in one panel with a synopsis of the information, including key performance parameters such as SNR and THD.

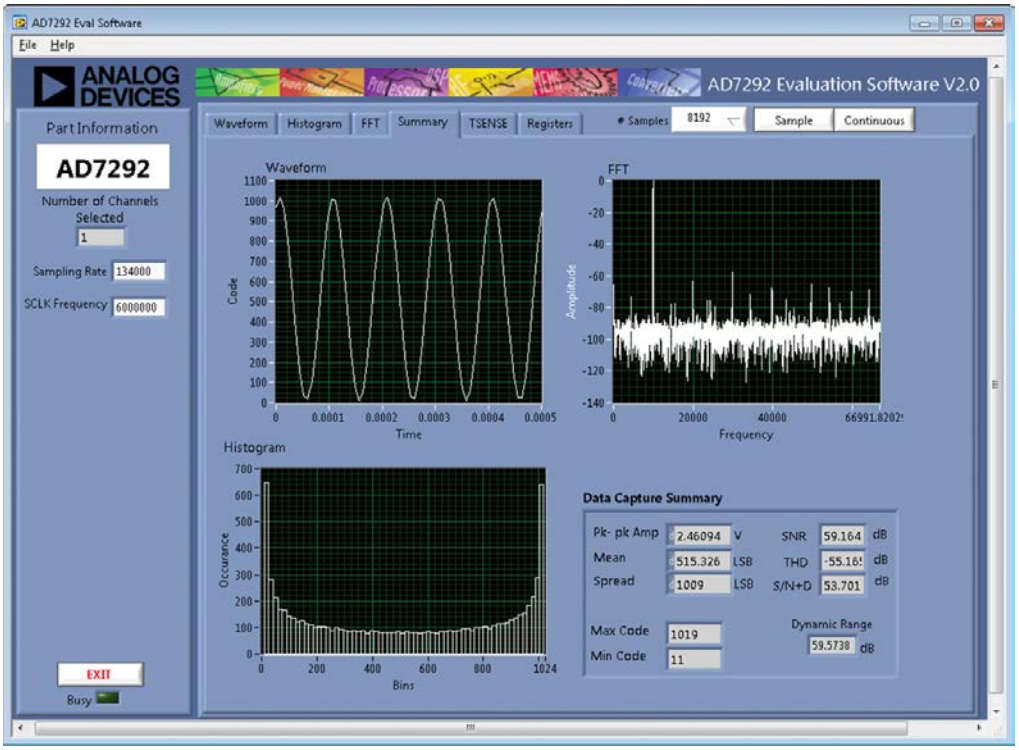

Figure 21. Summary Tab

Displaying Temperature Measurements

Figure 21 shows the **TSENSE** tab. There are two modes of operation (continuous and single sample), and the controls are located at the bottom of the panel.

Before temperature measurements can be displayed, the control bit must be set to active in the **Configuration Register Bank** (see Figure 23 and Figure 24). A digital filter can also be applied to this measurement.

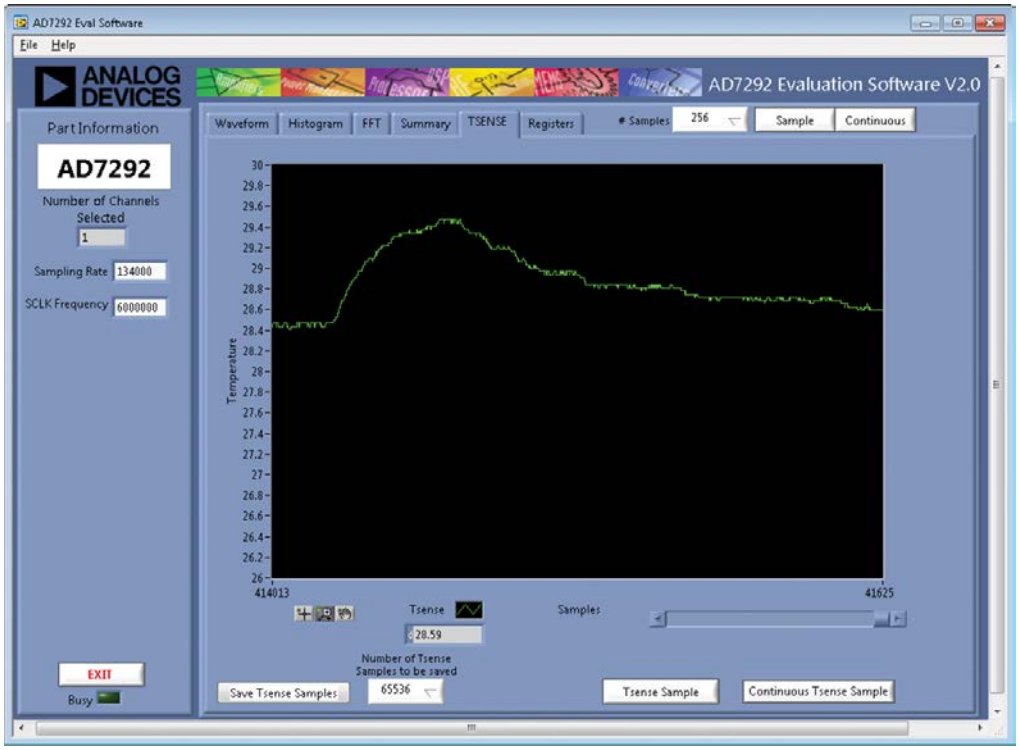

Figure 22. TSENSE Tab

Modifying Control Register Settings

Figure 23 shows the **Registers** tab. There are 87 registers used to configure the AD7292. Consult the AD7292 data sheet for a detailed explanation of each control register and an overview of the functions and features of the device.

The power-on default values for all registers are shown in Figure 24 to Figure 27.

For basic operation of the ADCs, it is not necessary to modify any of the registers directly. Provision is made on the **Waveform** tab (see Figure 18), which allows you to click **Enable** or **Disable** to select which input ADC channels are activated and to click **ON** to display the waveform of the input signal in the window.

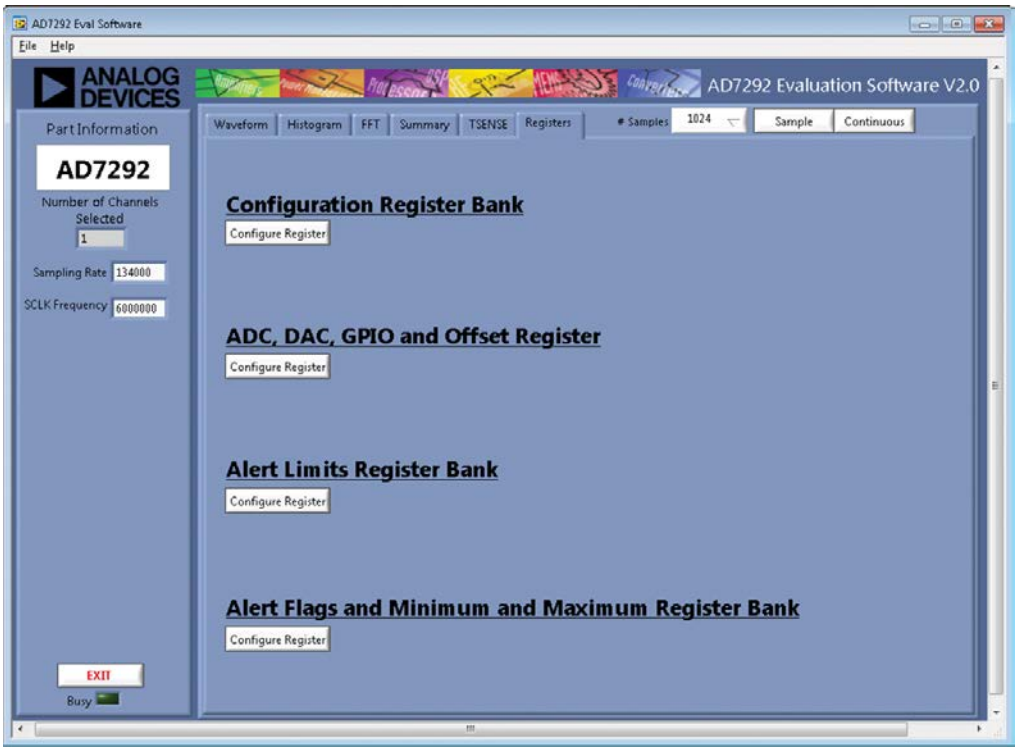

Figure 23. Registers Tab

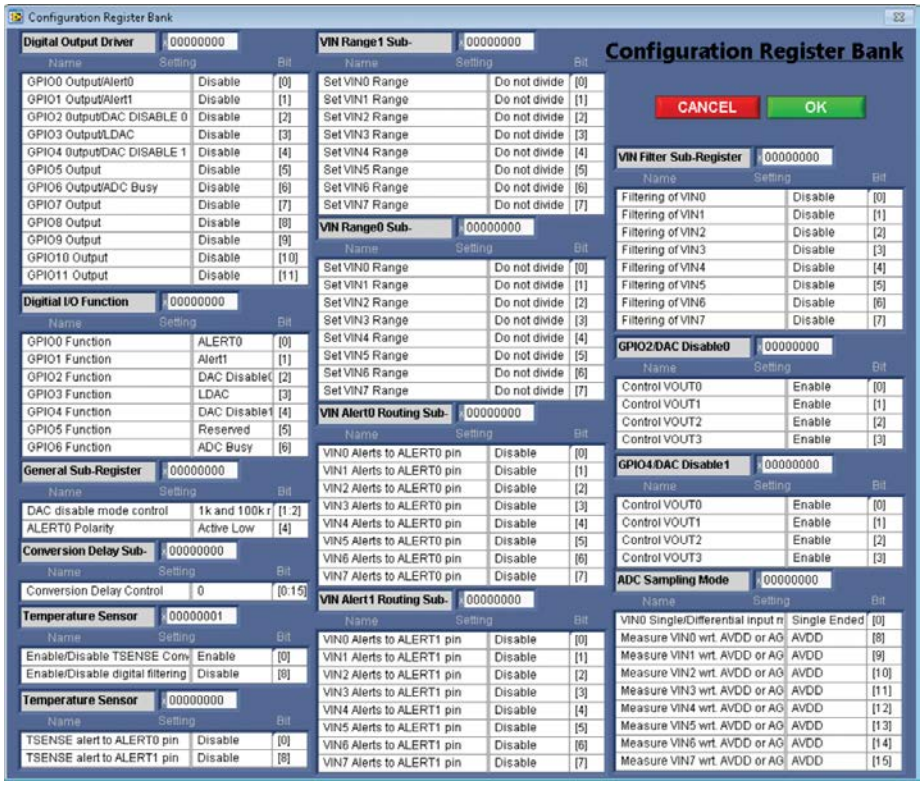

Figure 24. Configuration Register Bank Window

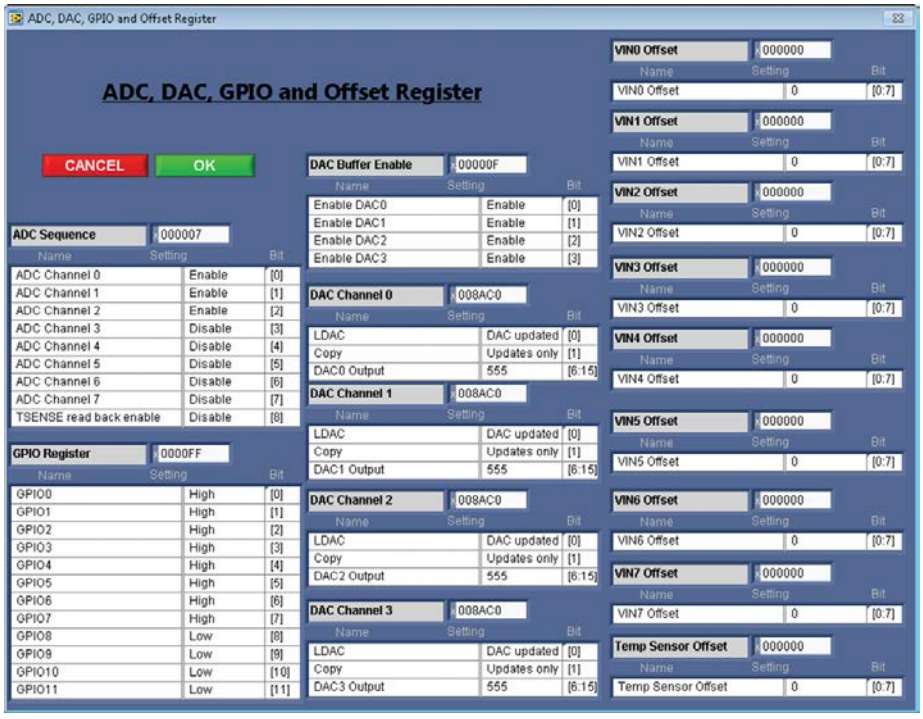

Figure 25. ADC, DAC, GPIO, and Offset Register Window

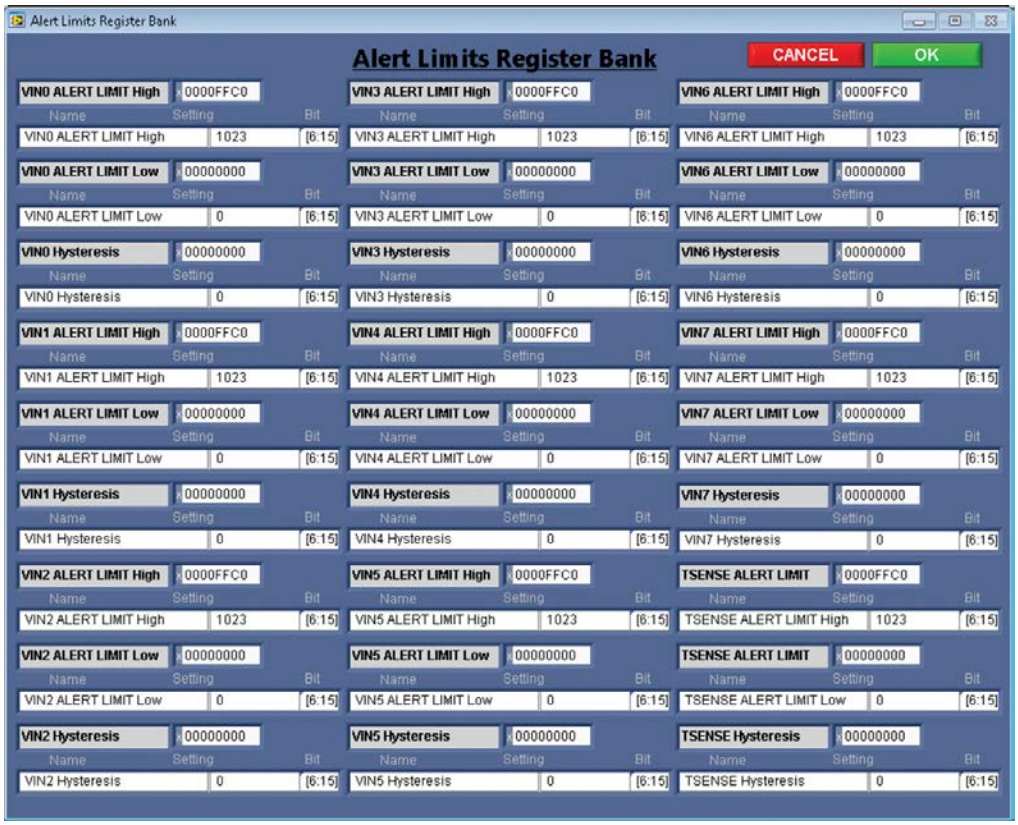

Figure 26. Alert Limits Register Bank Window

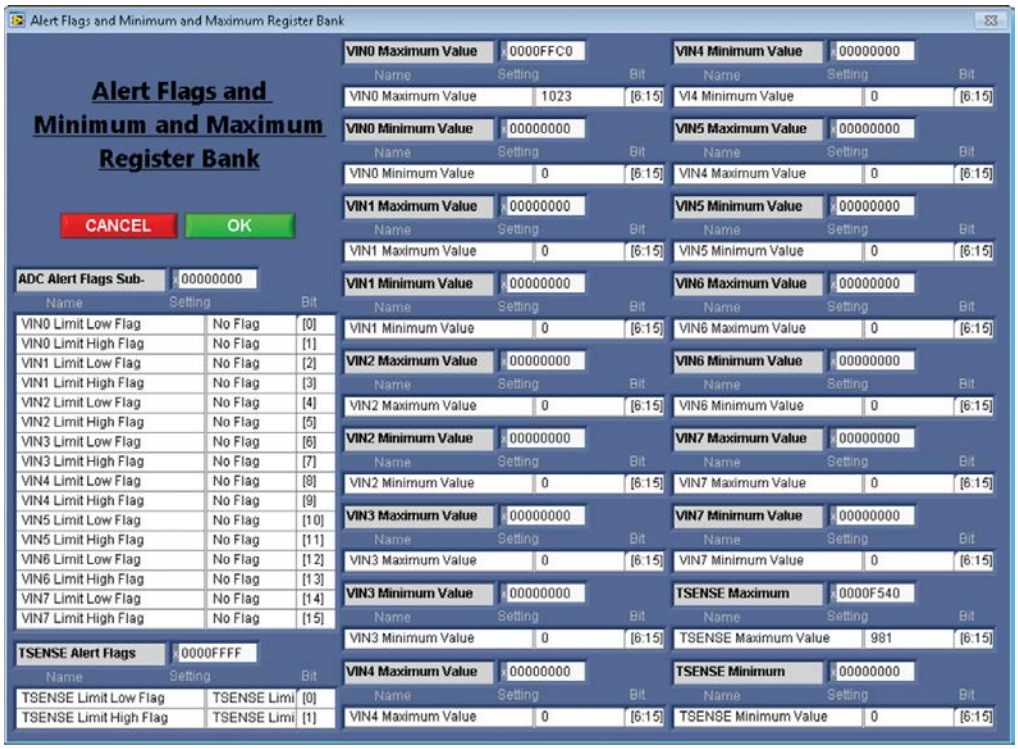

Figure 27. Alert Flags and Minimum and Maximum Register Bank Window

RELATED LINKS

Resource	Description
ADP170	Product Page, Low Dropout CMOS Linear Regulator
AD8066	Product Page, High Speed Low Noise Amplifier
EngineerZone	Online Community, Analog Devices Online Technical Support Community
Circuits from the Lab	Reference Circuits, Circuit Designs That Have Been Built and Tested to Ensure Function and Performance and That Address Common Analog, RF/IF, and Mixed-Signal Design Challenges by Applying Analog Devices' Vast Applications Expertise

NOTES

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ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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