PIC10F200/202/204/206

Memory Programming Specification

This document includes the programming specifications for the following devices:

- PIC10F200
- PIC10F202
- PIC10F204
- PIC10F206

1.0 PROGRAMMING THE PIC10F200/202/204/206

The PIC10F200/202/204/206 is programmed using a serial method. The Serial mode will allow the PIC10F200/202/204/206 to be programmed while in the user's system. This allows for increased design flexibility. This programming specification applies to PIC10F200/202/204/206 devices in all packages.

1.1 Hardware Requirements

The PIC10F200/202/204/206 requires one power supply for VDD (5.0V) and one for VPP (12V).

1.2 Program/Verify Mode

The Program/Verify mode for the PIC10F200/202/204/206 allows programming of user program memory for user ID locations, backup OSCCAL location and the Configuration Word.

Pin Diagrams

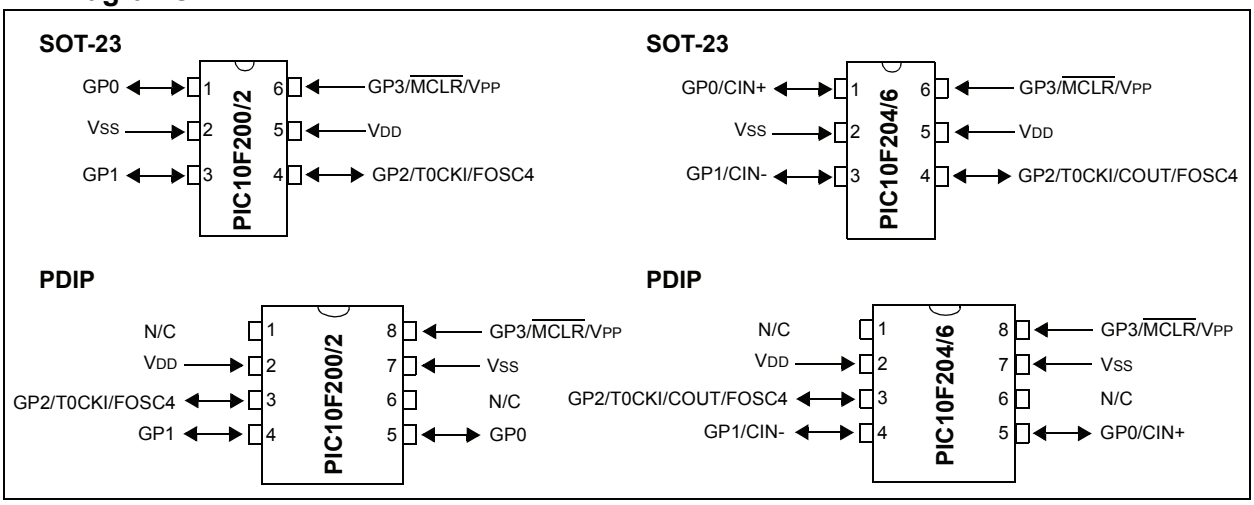


TABLE 1-1: PIN DESCRIPTIONS (DURING PROGRAMMING): PIC10F200/202/204/206

Pin Name	During Programming		
	Function	Pin Type	Pin Description
GP1	ICSPCLK	I	Clock input – Schmitt Trigger input
GP0	ICSPDAT	I/O	Data input/output – Schmitt Trigger input
MCLR/VPP	Program/Verify mode	P	Programming Power
VDD	VDD	P	Power Supply
VSS	VSS	P	Ground

Legend: I = Input, O = Output, P = Power

2.0 MEMORY MAPPING

2.1 User Program Memory Map

The user memory space extends from (0x000-0x0FF) on the PIC10F200/204 and (0x000-0x1FF) on the PIC10F202/206. In Program/Verify mode, the program memory space extends from (0x000-0x1FF) for the PIC10F200/204 and (0x000-0x3FF) for the PIC10F202/206. The first half, (0x000-0x0FF) and (0x000-0x1FF) respectively, is user program memory. The second half, (0x100-0x1FF) and (0x200-0x3FF) respectively, is configuration memory. The PC will increment from (0x000-0x0FF) and (0x000-0x1FF) respectively, then to 0x100 and 0x200, respectively (not to 0x000).

In the configuration memory space, 0x100-0x13F for the PIC10F200/204, and 0x200-0x23F for the PIC10F202/206, are physically implemented. However, only locations 0x100-0x103 and 0x200-0x203 are available. Other locations are reserved.

2.2 User ID Locations

A user may store identification information (ID) in four user ID locations. The user ID locations are mapped in [0x100:0x103] and [0x200:0x203], respectively. Each user ID location is 12 bits.

The contents of user ID locations are used in the calculation of the device checksum when Code Protection is enabled ($\overline{CP}$ = 0). The four Least Significant bits (LSbs) of each location are concatenated into a 2-byte value, the “User ID”, and used in the checksum calculation. This 2-byte “User ID” is displayed by MPLAB® IDE. Table 2-1 illustrates an example of the relationship between the user ID locations and the “User ID” value (PIC10F200/204), used in the checksum computations (see Table 5-1 and Table 5-2).

TABLE 2-1: “USER ID” VALUE AND LOCATION (PIC10F200/204 EXAMPLE)

User ID Memory Address	User ID Location – 12-bit value		“User ID” Values
	Binary	Hex	
0x100	0000 0000 1001b	009h	**9**xxxh
0x101	1100 0001 1000b	C18h	x**8**xxh
0x102	0111 0010 0100b	724h	xx**4**xh
0x103	0110 0011 0101b	635h	xxx**5**h

“User ID” composite value displayed in MPLAB IDE = 9845h

Although 12 bits are available in each location, previous devices only implemented the lower 4 bits of each location. As a result, these additional bits may not have support in the language and programming tools. For this reason, it is recommended that the user only use the four LSBs of each user ID location.

2.3 Configuration Word

The Configuration Word register is physically located at 0x1FF and 0x3FF, respectively. It is only available upon Program mode entry. Once an Increment Address command is issued, the Configuration Word is no longer accessible, regardless of the address of the program counter.

Note: By convention, the Configuration Word register is stored at the logical address location of 0xFFF within the hex file generated for the PIC10F200/202/204/206. This logical address location may not reflect the actual physical address for the part itself. It is the responsibility of the programming software to retrieve the Configuration Word register from the logical address within the hex file and translate the address to the proper physical location when programming.

FIGURE 2-2: PIC10F200/204 PROGRAM MEMORY MAP

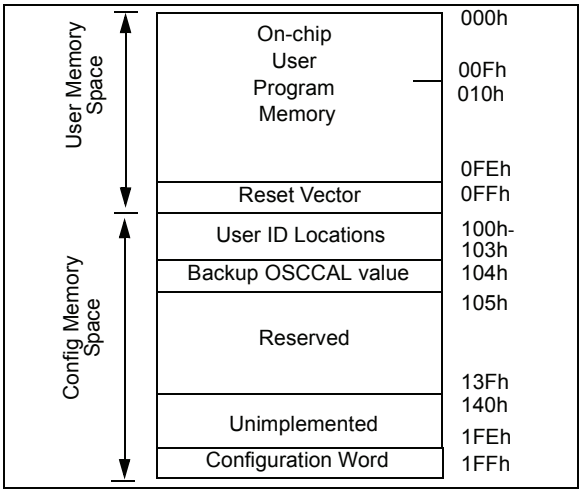
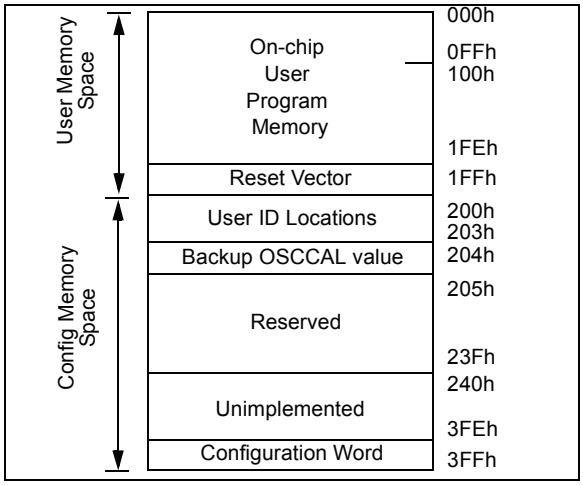


FIGURE 2-3: PIC10F202/206 PROGRAM MEMORY MAP



2.4 Oscillator Calibration Bits

The oscillator Calibration bits are stored at the Reset vector as the operand of a `MOVLW` instruction. Programming interfaces must allow users to program the Calibration bits themselves for custom trimming of the INTOSC. Capability for programming the Calibration bits when programming the entire memory array must also be maintained for backwards compatibility.

2.5 Backup OSCCAL Value

The backup OSCCAL value, 0x104/0x204, is a factory reserved location where the OSCCAL value is stored during testing of the INTOSC. This location is not erased during a standard Bulk Erase, but is erased if the PC is moved into configuration memory prior to invoking a Bulk Erase. If this value is erased, it is the user's responsibility to rewrite it back to this location for future use.

3.0 PROGRAM/VERIFY MODE

In Program/Verify mode, the program memory and the configuration memory can be accessed and programmed in serial fashion. ICSPDAT and ICSPCLK are used for the data and the clock, respectively. All commands and data words are transmitted LSb first. Data changes on the rising edge of the ICSPCLK and is latched on the falling edge. In Program/Verify mode, both the ICSPDAT and ICSPCLK are Schmitt Trigger inputs. The sequence that enters the device into Program/Verify mode places all other logic into the Reset state. Upon entering Program/Verify mode, all I/Os are automatically configured as high-impedance inputs and the address is cleared.

3.1 High-Voltage Program/Verify mode Entry and Exit

There are two different methods of entering Program/Verify mode via high-voltage:

- VDD- First Entry mode
- VPP- First Entry mode

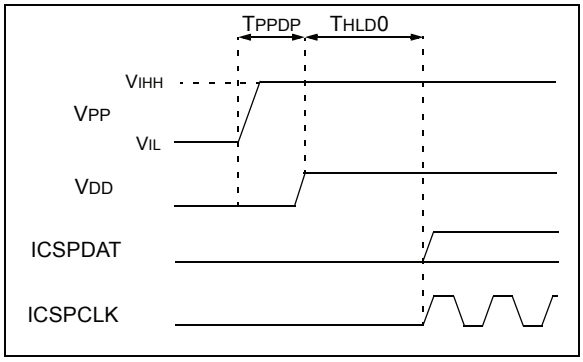
3.1.1 VPP- FIRST ENTRY MODE

To enter Program/Verify mode via the VPP- first method, please follow the sequence below:

1. Hold ICSPCLK and ICSPDAT low. All other pins should be un-powered.
2. Raise the voltage on $\overline{\text{MCLR}}$/VPP from 0V to VIHH.
3. Raise the voltage on VDD from 0V to the desired operating voltage.

The VPP- first entry prevents the device from executing code prior to entering Program/Verify mode. For example, when Configuration Word 1 has $\overline{\text{MCLR}}$ disabled (MCLRE = 0), the power-up time is disabled (PWRTE = 0), the internal oscillator is selected (FOSC = 100), and ICSPCLK and ICSPDAT pins are driven by the user application, the device will execute code. Since this may prevent entry, VPP- First Entry mode is strongly recommended. See the timing diagram in Figure 3-1.

FIGURE 3-1: PROGRAMMING MODE ENTRY – VPP FIRST



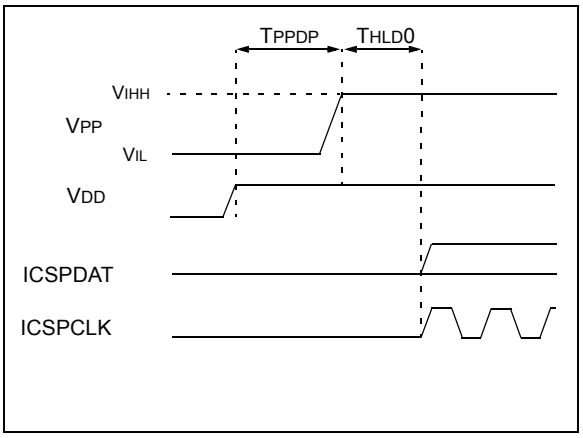
3.1.2 VDD- FIRST ENTRY MODE

To enter Program/verify mode via the VDD- first method, please follow the sequence below:

1. Hold ICSPCLK and ICSPDAT low.
2. Raise the voltage on VDD from 0V to the desired operating voltage (VIL to VDD).
3. Raise the voltage on $\overline{\text{MCLR}}$/VPP from VDD or below, to VIHH.

The VDD- first method is useful when programming the device when VDD is already applied, for it is not necessary to disconnect VDD to enter Program/Verify mode. See the timing diagram in Figure 3-2.

FIGURE 3-2: PROGRAMMING MODE ENTRY – VDD FIRST



3.1.3 PROGRAM/VERIFY MODE EXIT

To exit Program/Verify mode take $\overline{MCLR}$ to VDD or lower (VIL). See Figure 3-3 and Figure 3-4.

FIGURE 3-3: PROGRAMMING MODE EXIT – VPP LAST

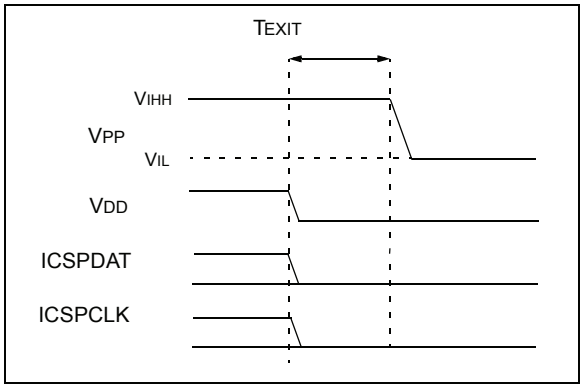
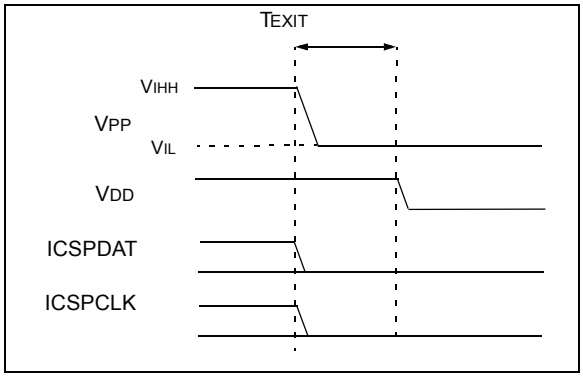


FIGURE 3-4: PROGRAMMING MODE EXIT – VDD LAST



3.2 Program/Verify Commands

The PIC® Flash MCUs programming commands are six bits in length. The commands are summarized in Table 3-1. Commands that have data associated with them are specified to have a minimum delay of TDLY between the command and the data. After this delay, 16 clocks are required to either clock in or clock out the 14-bit data word. The first clock is for the Start bit and the last clock is for the Stop bit.

3.2.1 SERIAL PROGRAM/VERIFY OPERATION

The ICSPCLK pin is used for clock input and the ICSPDAT pin is used for data input/output during serial operation. To input a command, the clock pin is cycled six times. Each command bit is latched on the falling edge of the clock with the LSb of the command being input first. The data must adhere to the setup (TSET1) and hold (THLD1) times with respect to the falling edge of the clock (see Table 6-1).

Commands that do not have data associated with them are required to wait a minimum of TDLY2 measured from the falling edge of the last command clock to the rising edge of the next command clock (see Table 6-1). Commands that do have data associated with them (Read and Load) are also required to wait TDLY2 between the command and the data segment measured from the falling edge of the last command clock to the rising edge of the first data clock. The data segment, consisting of 16 clock cycles, can begin after this delay.

Note:	After every End Programming command, a delay of TDIS is required.

The first and last clock pulses during the data segment correspond to the Start and Stop bits, respectively. Input data is a “don't care” during the Start and Stop cycles. The 14 clock pulses between the Start and Stop cycles clock the 14 bits of input/output data. Data is transferred LSb first.

During Read commands, in which the data is output from the PIC Flash MCUs, the ICSPDAT pin transitions from the high-impedance input state to the low-impedance output state at the rising edge of the second data clock (first clock edge after the Start cycle). The ICSPDAT pin returns to the high-impedance state at the rising edge of the 16th data clock (first edge of the Stop cycle). See Figure 3-6.

The commands that are available are described in Table 3-1.

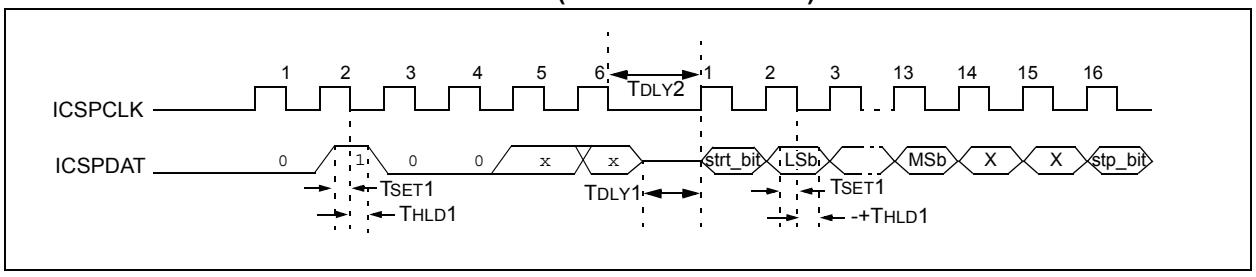
TABLE 3-1: COMMAND MAPPING FOR PIC10F200/202/204/206

Command	Mapping (MSb … LSb)						HEX	Data
Load Data for Program Memory	x	x	0	0	1	0	02h	0, data (14), 0
Read Data from Program Memory	x	x	0	1	0	0	04h	0, data (14), 0
Increment Address	x	x	0	1	1	0	06h	
Begin Programming	x	x	1	0	0	0	08h	Externally Timed
End Programming	x	x	1	1	1	0	0Eh	
Bulk Erase Program Memory	x	x	1	0	0	1	09h	Internally Timed

3.2.1.1 Load Data For Program Memory

After receiving this command, the chip will load in a 14-bit "data word" when 16 cycles are applied, as described previously. Because this is a 12-bit core, the two MSbs of the data word are ignored. A timing diagram for the Load Data command is shown in Figure 3-5.

FIGURE 3-5: LOAD DATA COMMAND (PROGRAM/VERIFY)

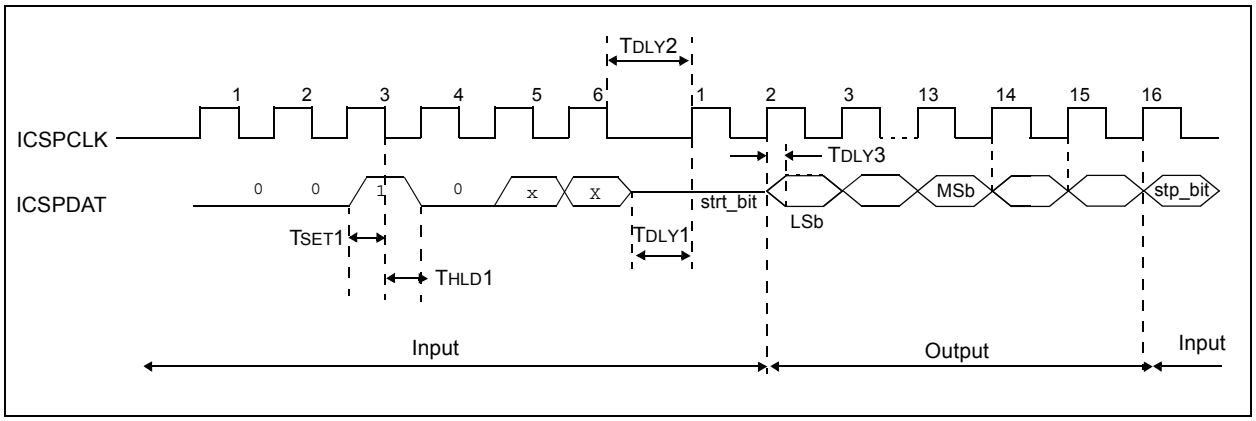


3.2.1.2 Read Data From Program Memory

After receiving this command, the chip will transmit data bits out of the program memory (user or configuration) currently addressed, starting with the second rising edge of the clock input. The data pin will go into Output mode on the second rising clock edge, and it will revert to Input mode (high-impedance) after the 16th rising edge. Because this is a 12-bit core, the two MSbs of the 14-bit word will be read as '0's.

If the program memory is code-protected ($\overline{CP}$ = 0), portions of the program memory will be read as zeros. See **Section 5.0 "Code Protection"** for details.

FIGURE 3-6: READ DATA FROM PROGRAM MEMORY COMMAND

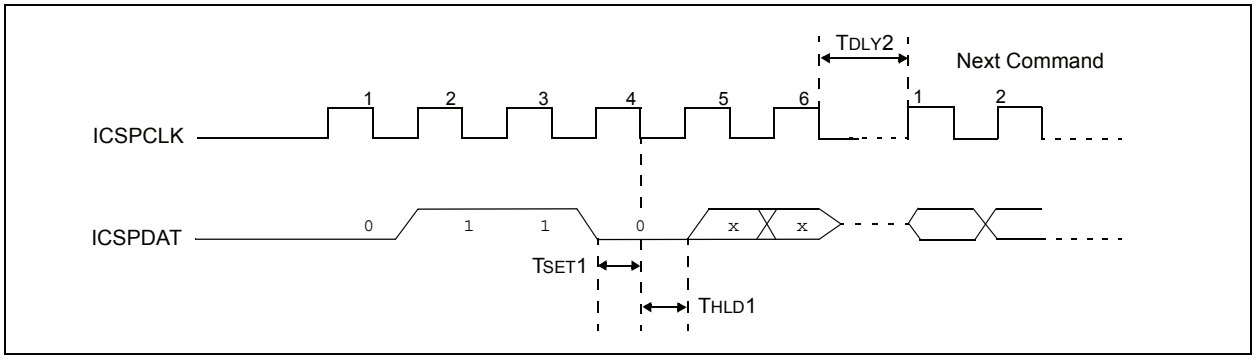


3.2.1.3 Increment Address

The PC is incremented when this command is received. A timing diagram of this command is shown in Figure 3-7.

It is not possible to decrement the address counter. To reset this counter, the user must either exit and re-enter Program/Verify mode or increment the PC from 0x1FF for the PIC10F200/204 or 0x3FF for the PIC10F202/206 to 0x000.

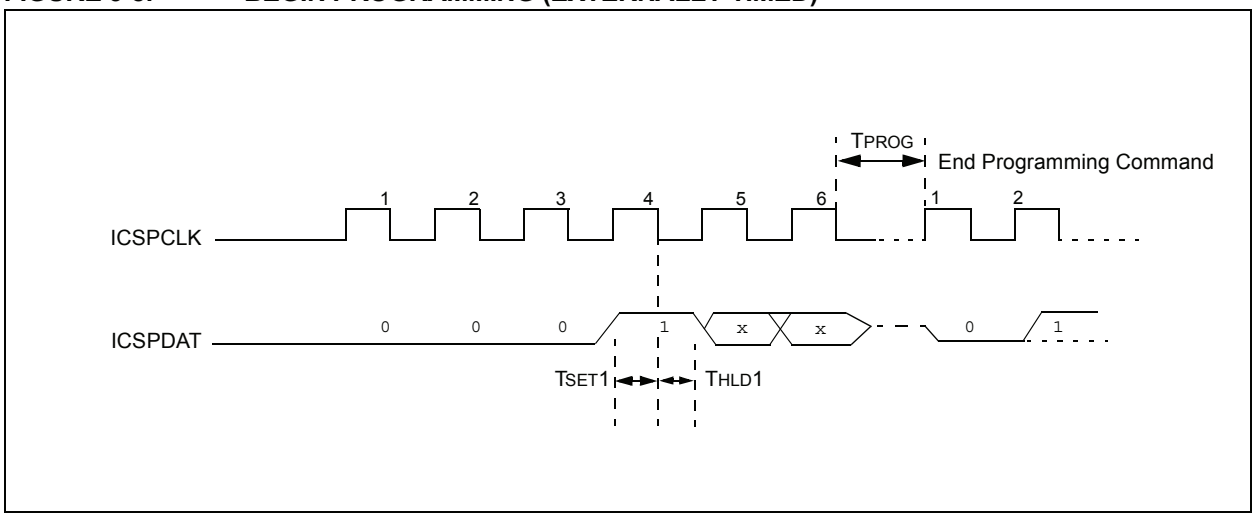
FIGURE 3-7: INCREMENT ADDRESS COMMAND



3.2.1.4 Begin Programming (Externally Timed)

A Load command must be given before every Begin Programming command**.** Programming will begin after this command is received and decoded. Programming requires (TPROG) time and is terminated using an End Programming command. This command programs the current location, no erase is performed.

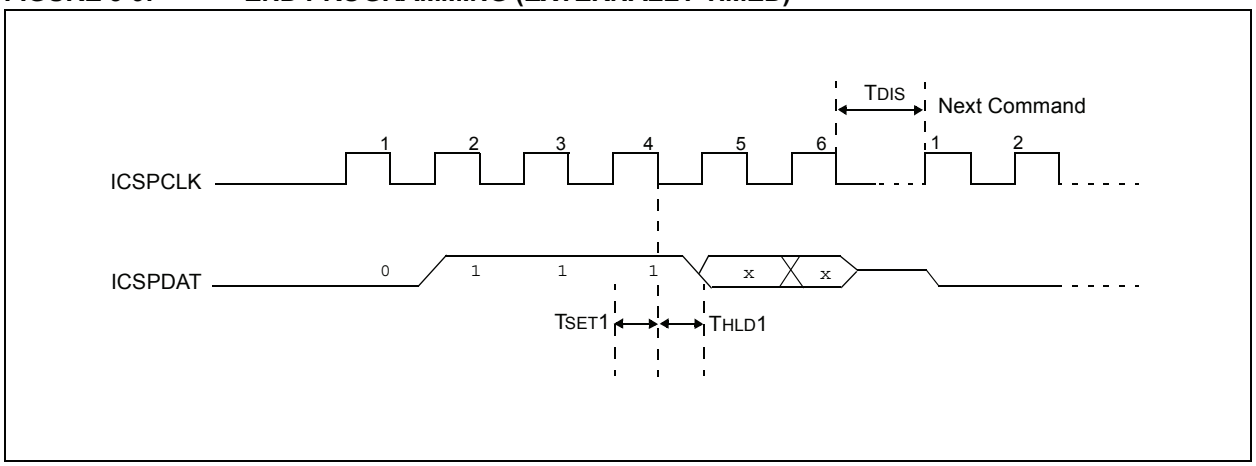
FIGURE 3-8: BEGIN PROGRAMMING (EXTERNALLY TIMED)



3.2.1.5 End Programming

The End Programming command terminates the program process. A delay of TDIS (see Table 6-1) is required before the next command to allow the internal programming voltage to discharge (see Figure 3-9).

FIGURE 3-9: END PROGRAMMING (EXTERNALLY TIMED)



3.2.1.6 Bulk Erase Program Memory

After this command is performed, the entire program memory and Configuration Word is erased.

Note 1:	A fully erased part will read '1's in every program memory location.
2:	The oscillator Calibration bits are erased if a Bulk Erase is invoked. They must be read and saved prior to erasing the device and restored during the programming operation. Oscillator Calibration bits are stored at the Reset vector as the operand of a MOVLW instruction.

To perform a Bulk Erase of the program memory and configuration fuses, the following sequence must be performed (see Figure 3-15).

1. Read and save 0x0FF/0x1FF oscillator Calibration bits and 0x104/0x204 backup OSCCAL bits into computer/programmer temporary memory.
2. Enter Program/Verify mode. PC is set to Configuration Word address.
3. Perform a Bulk Erase Program Memory command.
4. Wait TERA to complete Bulk Erase.
5. Restore OSCCAL bits.

To perform a full device Bulk Erase of the program memory, configuration fuses, user IDs and backup OSCCAL value, the following sequence must be performed (see Figure 3-16).

1. Read and save 0x0FF/0x1FF oscillator Calibration bits and 0x104/0x204 backup OSCCAL bits into computer/programmer temporary memory.
2. Enter Program/Verify mode.
3. Increment PC to 0x200/0x400 (first user ID location).
4. Perform a Bulk Erase command.
5. Wait TERA to complete Bulk Erase.
6. Restore OSCCAL bits.
7. Restore backup OSCCAL bits.

TABLE 3-2: BULK ERASE RESULTS

PC =	Program Memory Space		Configuration Memory Space		
	Program Memory	Reset Vector	Configuration Word	User ID	Backup OSCCAL
Configuration Word or Program Memory Space	E	E	E	U	U
First User ID Location	E	E	E	E	E

FIGURE 3-10: BULK ERASE PROGRAM MEMORY COMMAND

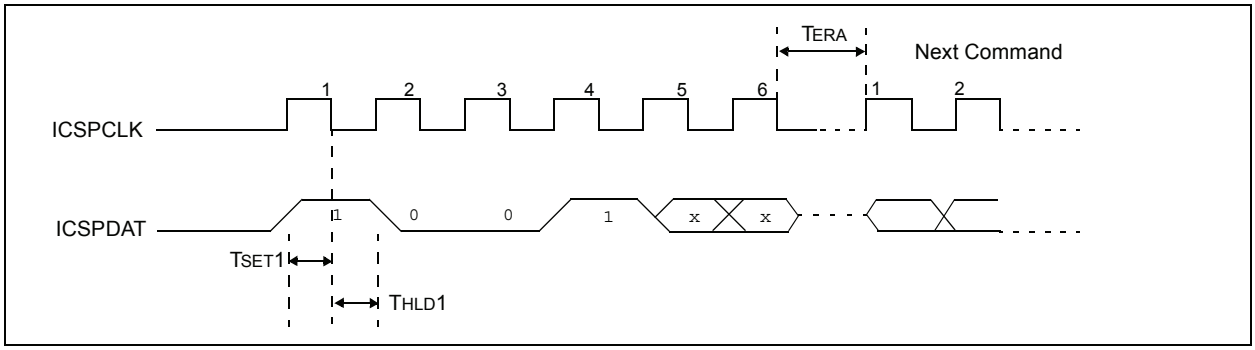


FIGURE 3-11: READING AND TEMPORARY SAVING OF THE OSCCAL CALIBRATION BITS

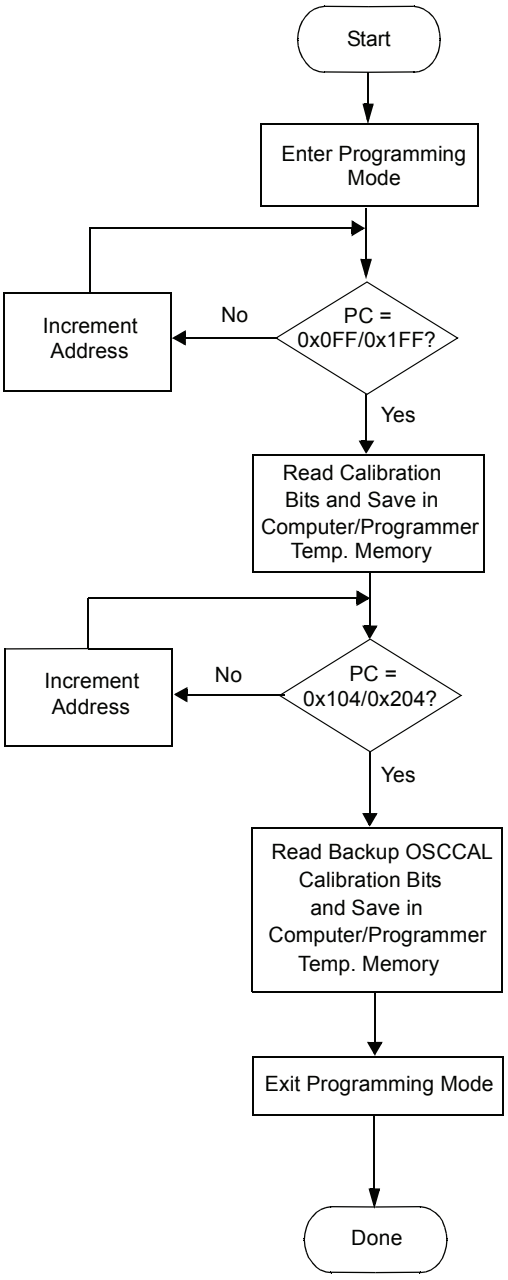


FIGURE 3-12: RESTORING/PROGRAMMING THE OSCCAL CALIBRATION BITS

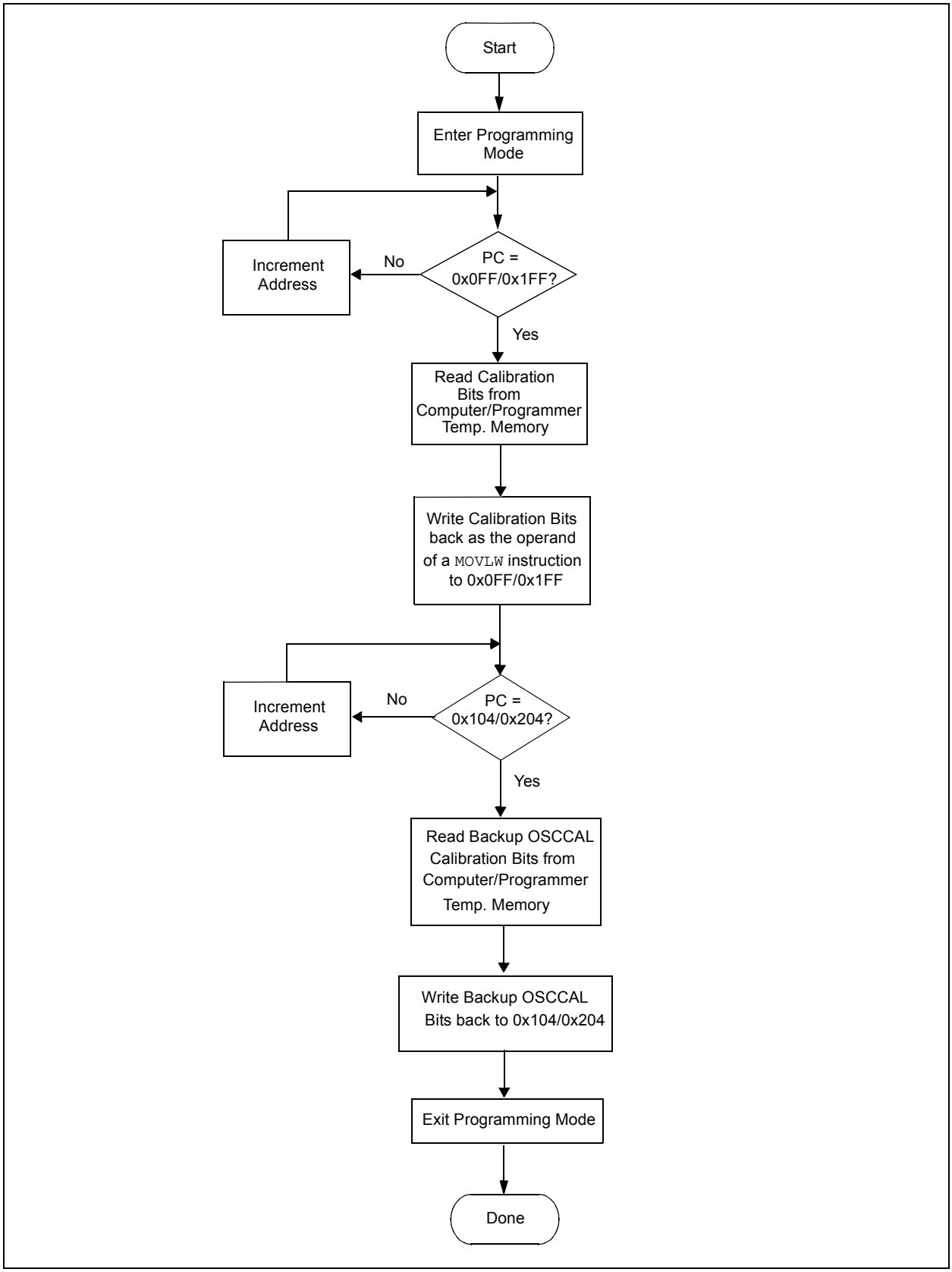


FIGURE 3-13: PROGRAM FLOW CHART – PIC10F200/202/204/206 PROGRAM MEMORY

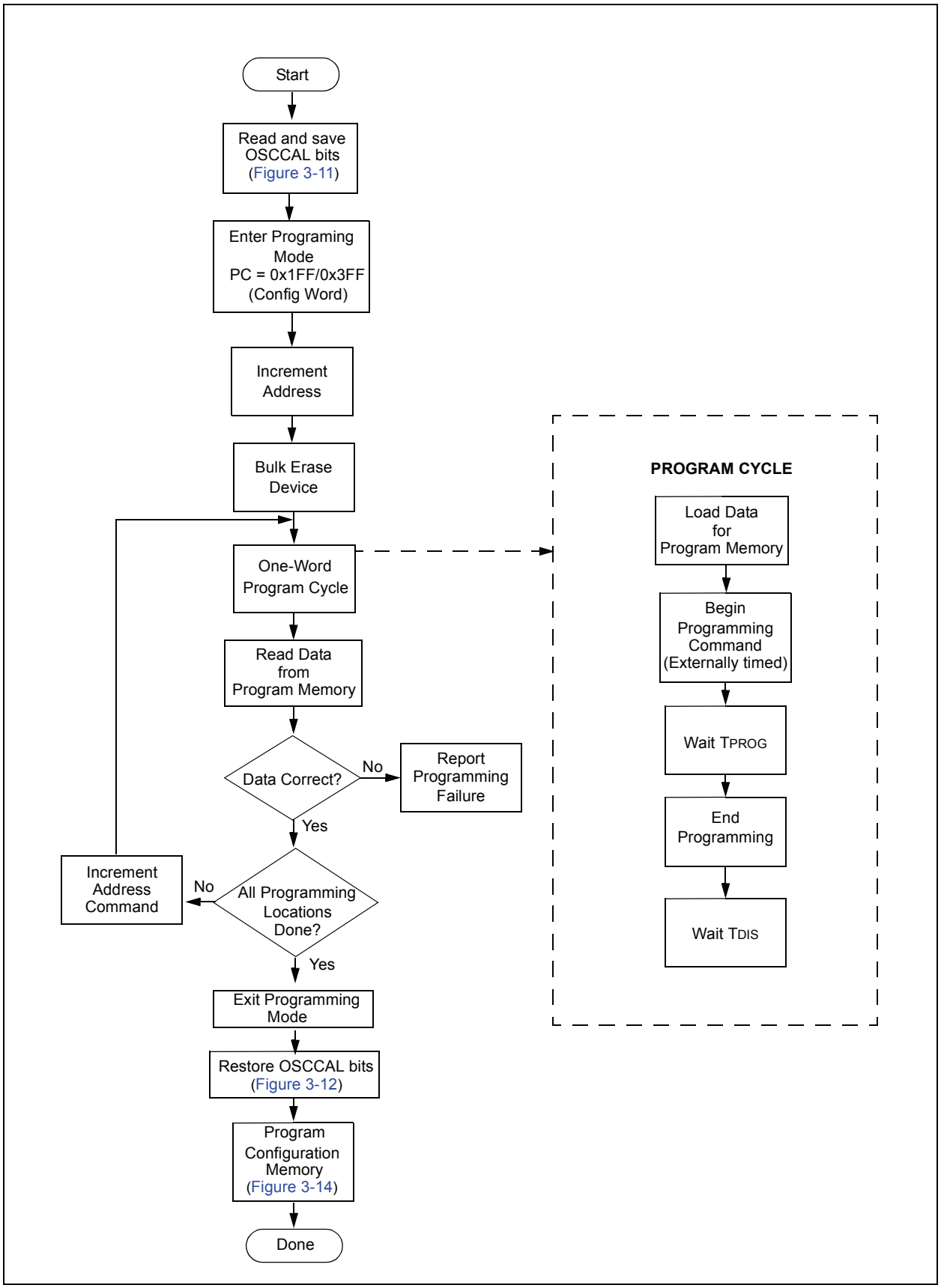


FIGURE 3-14: PROGRAM FLOW CHART – PIC10F200/202/204/206 CONFIGURATION MEMORY

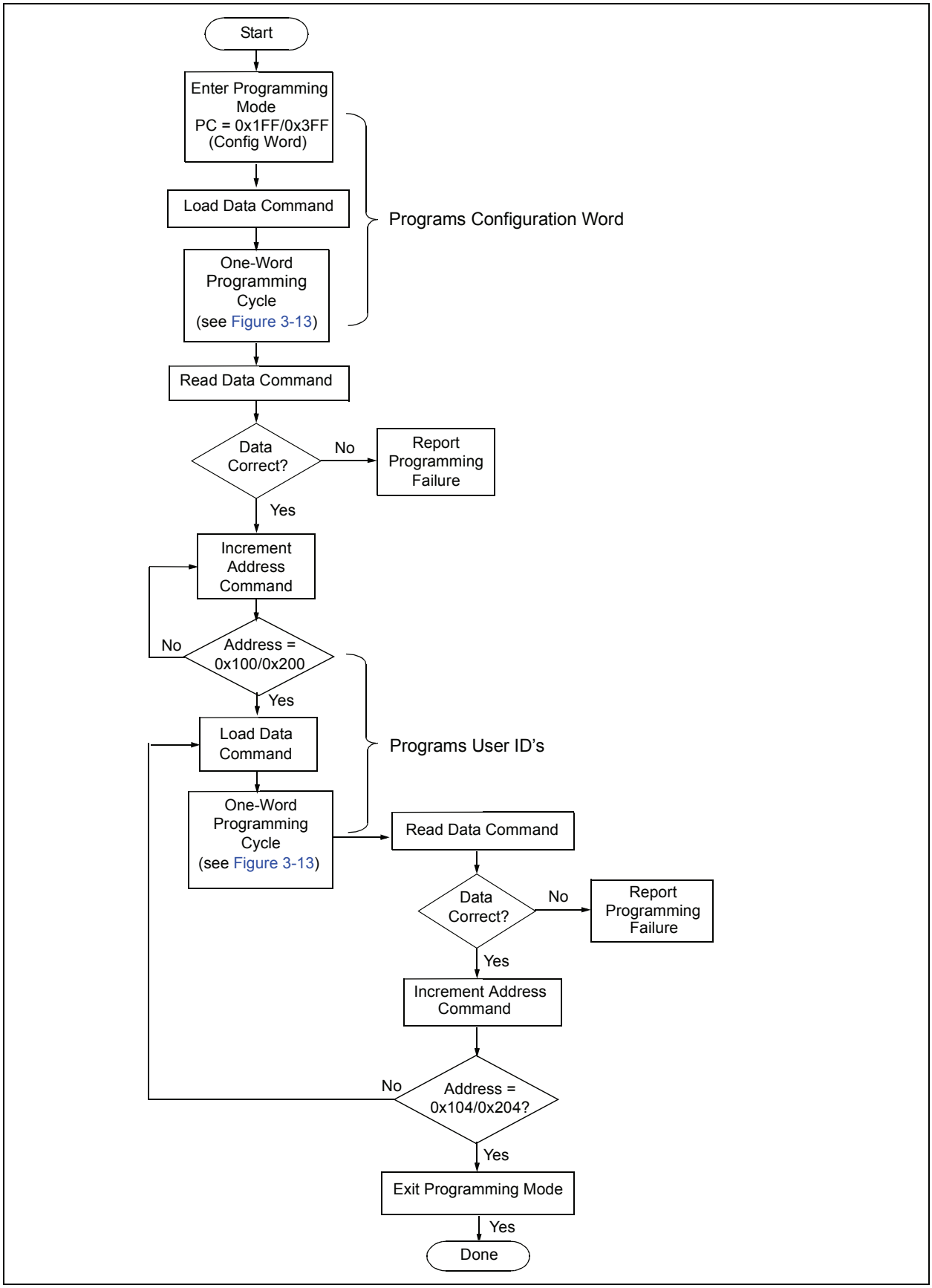


FIGURE 3-15: PROGRAM FLOW CHART – ERASE PROGRAM MEMORY, CONFIGURATION WORD

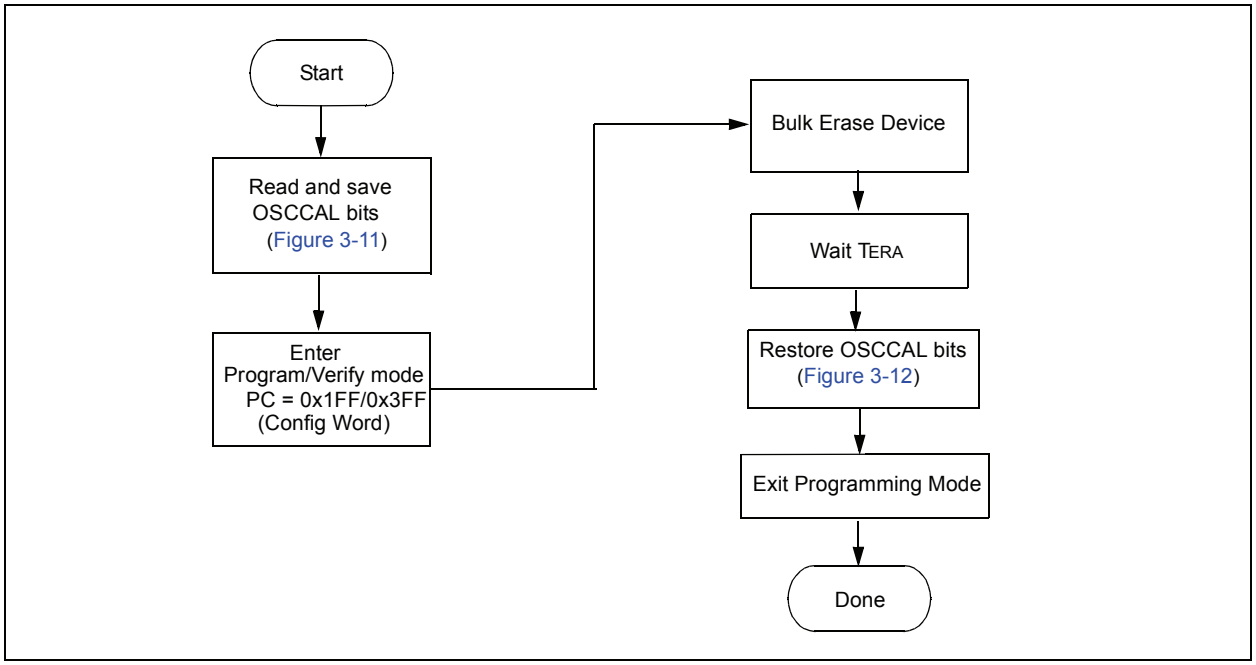
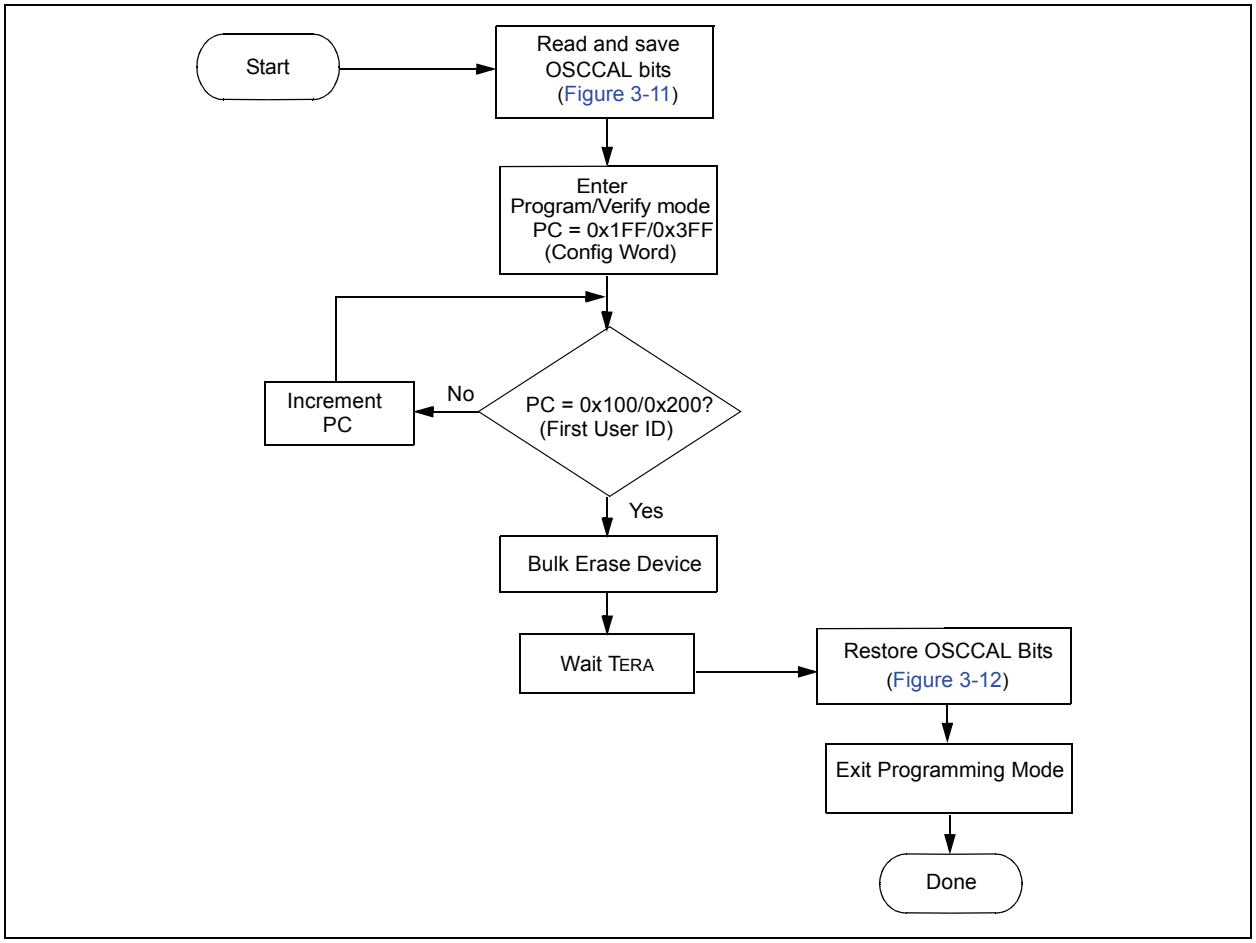


FIGURE 3-16: PROGRAM FLOW CHART – ERASE PROGRAM MEMORY, CONFIGURATION WORD AND USER ID



4.0 CONFIGURATION WORD

The PIC10F200/202/204/206 has several Configuration bits. These bits can be programmed (reads '0') or left unchanged (reads '1'), to select various device configurations.

REGISTER 4-1: CONFIGURATION WORD – PIC10F200/202/204/206

U-1	U-1	U-1	U-1
—	—	—	—
bit 11			bit 8

U-1	U-1	U-1	R/P-1	R/P-1	R/P-1	U-1	U-1
—	—	—	MCLRE	$\overline{CP}$	WDTE	—	—
bit 7							bit 0

Legend:	W = Writable bit	'0' = Bit is cleared
R = Readable bit	'1' = Bit is set	x = Bit is unknown
-n = Value at POR	U = Unimplemented bit	P = Programmable Bit

bit 11-5 **Unimplemented:** Read as '1'

bit 4 **MCLRE:** Master Clear Enable bit
1 = GP3/$\overline{MCLR}$ pin functions as $\overline{MCLR}$
0 = GP3/$\overline{MCLR}$ pin functions as GP3, $\overline{MCLR}$ internally tied to V_{DD}

bit 3 **$\overline{CP}$:** Code Protection bit
1 = Code protection off
0 = Code protection on

bit 2 **WDTE:** Watchdog Timer Enable bit
1 = WDT enabled
0 = WDT disabled

bit 1-0 **Unimplemented:** Read as '1'

5.0 CODE PROTECTION

For the PIC10F200/202/204/206, once code protection is enabled, all program memory locations, 0x040-0x0FE (F200/204) and 0x040-x1FE (F202/206) inclusive, read all '0's. Program memory locations, 0x000-0x03F, 0x0FF (F200/204) and 0x1FF (F202/206), are always unprotected. The user ID locations, backup OSCCAL locations, and the Configuration Word read out in an unprotected fashion. It is possible to program the user ID locations, backup OSCCAL locations and the Configuration Word after code-protect is enabled.

5.1 Disabling Code Protection

It is recommended that the following procedure be performed before any other programming is attempted. It is also possible to turn code protection off ($\overline{CP}$ = 1) using this procedure. However, *all data within the program memory will be erased when this procedure is executed, and thus, the security of the code is not compromised.*

To disable code-protect:

a) Enter Program mode.
b) Execute Bulk Erase Program Memory command (001001).
c) Wait TERA.

5.2 Embedding Configuration Word and User ID Information in the Hex File

Note:	To allow portability of code, the programmer is required to read the Configuration Word and user ID locations from the hex file when loading the hex file. If Configuration Word information was not present in the hex file, then a simple warning message may be issued. Similarly, while saving a hex file, Configuration Word and user ID information must be included. An option to not include this information may be provided. Microchip Technology Incorporated feels strongly that this feature is important for the benefit of the end customer.

5.3 Checksum Computation

5.3.1 CHECKSUM

The checksum is calculated by reading the contents of the PIC10F200/202/204/206 memory locations and adding up the opcodes up to the maximum user addressable location (e.g., 0x1FF for the PIC10F202/206). Any Carry bits exceeding 16 bits are neglected. Finally, the Configuration Word (appropriately masked) is added to the checksum. Checksum computation for the PIC10F200/202/204/206 is shown in Table 5-2.

The checksum is calculated by summing the following:

- The contents of all program memory locations
- The Configuration Word, appropriately masked
- Masked user ID locations (when applicable)

The Least Significant 16 bits of this sum is the checksum.

The following table describes how to calculate the checksum for each device.

Note:	The checksum calculation differs depending on the code-protect setting. The Configuration Word and user ID locations can always be read regardless of the code-protect settings.

TABLE 5-1: CHECKSUM COMPUTATIONS – PIC10F200/204

Device	Code-Protect	Checksum*	Blank Value	0x723 at 0 and Max Address
PIC10F200/204	OFF	SUM[0x000:0x0FE] + CFGW & 0x01C	0xEF1D	0xDD65
	ON	SUM[0x00:0x3F] + CFGW & 0x01C + SUM_ID(1)	0xEEF1	0xD45D

Legend: CFGW = Configuration Word
SUM[a:b] = [Sum of locations a to b inclusive]
SUM_ID = User ID locations masked by 0x00F then made into a 16-bit value with ID0 as the Most Significant nibble.
For example, ID0 = 0x1, ID1 = 0x2, ID2 = 0x3, ID3 = 0x4, then SUM_ID = 0x1234.
*Checksum = [Sum of all the individual expressions] & [0x0FFFF]
+ = Addition
& = Bitwise AND

Note 1: The checksum shown assumes that SUM_ID contains the unprotected checksum.

TABLE 5-2: CHECKSUM COMPUTATIONS – PIC10F202/206

Device	Code-Protect	Checksum*	Blank Value	0x723 at 0 and Max Address
PIC10F202/206	OFF	SUM[0x000:0x1FE] + CFGW & 0x01C	0xEE1D	0xDC65
	ON	SUM[0x00:0x3F] + CFGW & 0x01C + SUM_ID(1)	0xEDF1	0xD35D

Legend: CFGW = Configuration Word
SUM[a:b] = [Sum of locations a to b inclusive]
SUM_ID = User ID locations masked by 0x00F then made into a 16-bit value with ID0 as the Most Significant nibble.
For example, ID0 = 0x1, ID1 = 0x2, ID2 = 0x3, ID3 = 0x4, then SUM_ID = 0x1234.
*Checksum = [Sum of all the individual expressions] & [0x0FFFF]
+ = Addition
& = Bitwise AND

Note 1: The checksum shown assumes that SUM_ID contains the unprotected checksum.

6.0 PROGRAM/VERIFY MODE ELECTRICAL CHARACTERISTICS

TABLE 6-1: AC/DC CHARACTERISTICS TIMING REQUIREMENTS FOR PROGRAM/VERIFY MODE

AC/DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise stated) Operating Temperature 10°C ≤ TA ≤ 40°C Operating Voltage 4.5V ≤ VDD ≤ 5.5V				
Sym.	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions/ Comments**
General						
VDDPROG	VDD level for programming operations, program memory	4.5	—	5.5	V	
VDDERA	VDD level for Bulk Erase operations, program memory	4.5	—	5.5	V	
IDDPROG	IDD level for programming operations, program memory	—	—	0.5	mA	
IDDERA	IDD level for Bulk Erase operations, program memory	—	—	0.5	mA	
VPP	High voltage on $\overline{MCLR}$ for Program/Verify mode entry	12.5	—	13.5	V	
IPP	$\overline{MCLR}$ pin current during Program/Verify mode	—	—	0.45	mA	
TVHHR	$\overline{MCLR}$ rise time (VSS to VIHH) for Program/ Verify mode entry	—	—	1.0	μs	
TPPDP	Hold time after VPP↑	5	—	—	μs	
TEXIT	Time delay when exiting Program/Verify mode	1	—	—	μs	
VIH1	(ICSPCLK, ICSPDAT) input high level	0.8 VDD	—	—	V	
VIL1	(ICSPCLK, ICSPDAT) input low level	—	—	0.2 VDD	V	
TSET0	ICSPCLK, ICSPDAT setup time before $\overline{MCLR}$↑ (Program/Verify mode selection pattern setup time)	100	—	—	ns	
THLD0	ICSPCLK, ICSPDAT hold time after $\overline{MCLR}$↑ (Program/Verify mode selection pattern setup time)	5	—	—	μs	
Serial Program/Verify						
TSET1	Data in setup time before clock↓	100	—	—	ns	
THLD1	Data in hold time after clock↓	100	—	—	ns	
TDLY1	Data input not driven to next clock input (delay required between command/data or command/command)	1.0	—	—	μs	
TDLY2	Delay between clock↓ to clock↑ of next command or data	1.0	—	—	μs	
TDLY3	Clock↑ to data out valid (during Read Data)		—	80	ns	
TERA	Erase cycle time	—	6	10(1)	ms	
TPROG	Programming cycle time (externally timed)	—	1	2(1)	ms	
TDIS	Time delay for internal programming voltage discharge	100	—	—	μs	
TRESET	Time between exiting Program mode with VDD and VPP at GND and then re-entering Program mode by applying VDD.	—	10	—	ms	

Note 1: Minimum time to ensure that function completes successfully over voltage, temperature and device variations.

APPENDIX A: REVISION HISTORY

Revision F (11/2011)

Revised Sections 2.2; 3.0-3.2; Table 3-1; Register 4-1; Table 5-1; Added Revision History.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
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