

# DATA SHEET

## **TDA8424**

Hi-Fi stereo audio processor;  
I<sup>2</sup>C-bus

Product specification  
File under Integrated Circuits, IC02

September 1992

Hi-Fi stereo audio processor; I<sup>2</sup>C-bus

TDA8424



## FEATURES

- Mode selector
- Spatial stereo, stereo and forced mono switch
- Volume and balance control
- Bass, treble and mute control
- Power supply with power-on reset

## GENERAL DESCRIPTION

The TDA8424 is monolithic bipolar integrated stereo sound circuit with a loudspeaker channel facility, digitally controlled via the I<sup>2</sup>C-bus for application in hi-fi audio and television sound.

## QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V <sub>CC</sub>	positive supply voltage (pin 4)	10.8	12.0	13.2	V
V <sub>I</sub>	input signal handling	2	–	–	V
V <sub>i</sub>	input sensitivity with full power at the output stage	–	300	–	mV
(S+N)/N	signal plus noise-to-noise ratio	–	86	–	dB
THD	total harmonic distortion	–	0.05	–	%
α <sub>cs</sub>	channel separation	–	80	–	dB
G <sub>vol</sub>	volume control range	–64	–	+6	dB
G <sub>tre</sub>	treble control range	–12	–	+12	dB
G <sub>bass</sub>	bass control range	–12	–	+15	dB

## ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8424	20	DIL	plastic	SOT146 <sup>(1)</sup>

## Note

1. SOT146-1; 1996 December 3.

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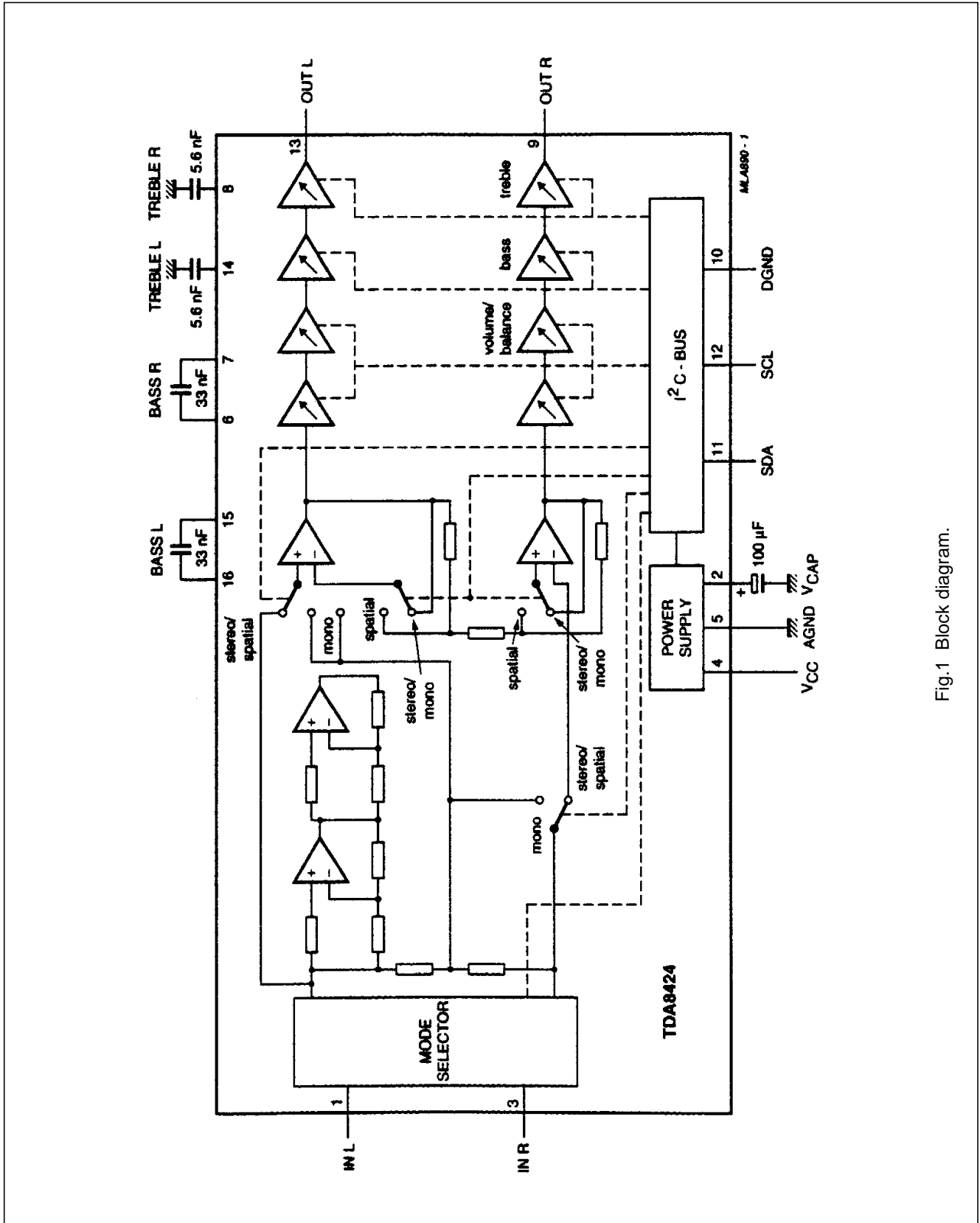
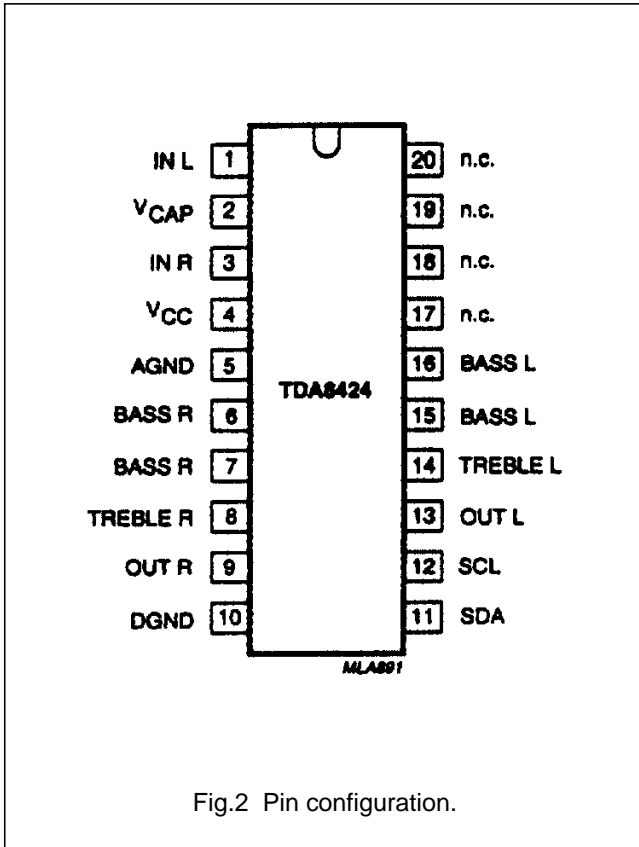


Fig.1 Block diagram.

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PINNING



SYMBOL	PIN	DESCRIPTION
IN L	1	left channel input
V <sub>CAP</sub>	2	decoupling capacitor
IN R	3	right channel input
V <sub>CC</sub>	4	positive supply voltage
AGND	5	analog ground
BASS R	6	right channel bass control
BASS R	7	right channel bass control
TREBLE R	8	right channel treble control
OUT R	9	right channel output
DGND	10	digital ground
SDA	11	serial data input/output
SCL	12	serial clock input
OUT L	13	left channel output
TREBLE L	14	left channel treble control
BASS L	15	left channel bass control
BASS L	16	left channel bass control
n.c.	17	not connected
n.c.	18	not connected
n.c.	19	not connected
n.c.	20	not connected

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**FUNCTIONAL DESCRIPTION****Mode selector**

The mode selector selects between stereo, sound A and sound B (in the event of bi-lingual transmission) for OUT R and OUT L.

**Volume control and balance**

The volume control consists of two stages (left and right). In each part the gain can be adjusted between +6 dB and -64 dB in steps of 2 dB. An additional step allows an attenuation of  $\geq 80$  dB. Both parts can be controlled independently over the whole range, which allows the balance to be varied by controlling the volume of left and right output channels.

**Stereo, spatial stereo and forced mono mode**

It is possible to select three modes: stereo, spatial stereo or forced mono. The spatial stereo mode handles stereo transmissions and the forced mono can be used in the event of stereo signals.

**Bass control**

The bass control can be switched from an emphasis of 15 dB to an attenuation of 12 dB for low frequencies in steps of 3 dB.

**Treble control**

The treble control stage can be switched from +12 dB to -12 dB in steps of 3 dB.

**Bias and power supply**

The TDA8424 includes a bias and power supply stage, which generates a voltage of  $0.5 V_{CC}$  with a low output impedance and injector currents for the logic part.

**Power-on reset**

The on-chip power-on reset circuit sets the mute bit to active, which mutes both parts of the treble amplifier. The muting can be switched by transmission of the mute bit.

**I<sup>2</sup>C-bus receiver and data handling****BUS SPECIFICATION**

The TDA8424 is controlled via the 2-wire I<sup>2</sup>C-bus by a microcontroller.

The two wires (SDA - serial data, SCL - serial clock) carry information between the devices connected to the bus.

Both SDA and SCL are bi-directional lines, connected to a

positive supply voltage via a pull-up resistor.

When the bus is free both lines are HIGH.

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock on the SCL line is LOW.

The set-up and hold times are specified in the AC CHARACTERISTICS.

A HIGH-to-LOW transition of the SDA line while SCL is HIGH is defined as a start condition.

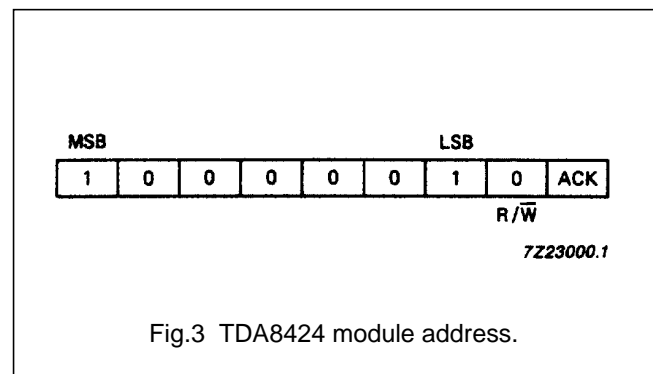
A LOW-to-HIGH transition of the SDA line while SCL is HIGH is defined as a stop condition.

The bus receiver will be reset by the reception of a start condition. The bus is considered to be busy after the start condition.

The bus is considered free again after a stop condition.

**Module address**

Data transmission to the TDA8424 starts with the module address MAD.

**Subaddress**

After the module address byte a second byte is used to select the following functions:

- Volume left, volume right, bass, treble and switch functions

The subaddress SAD is stored within the TDA8424. Table 1 defines the coding of the second byte after the module address MAD.

The automatic increment feature of the slave address enables a quick slave receiver initialization, within one transmission, by the I<sup>2</sup>C-bus controller (see Fig.5).

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**Table 1** Second byte after module address MAD

FUNCTION	128	64	32	16	8	4	2	1
	MSB				LSB			
	7	6	5	4	3	2	1	0
Volume left	0	0	0	0	0	0	0	0
Volume right	0	0	0	0	0	0	0	1
Bass	0	0	0	0	0	0	1	0
Treble	0	0	0	0	0	0	1	1
	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	0
Switch functions	0	0	0	0	1	0	0	0
					subaddress SAD			

**Definition of 3rd byte**

A third byte is used to transmit data to the TDA8424. Table 2 defines the coding of the third byte after module address MAD and subaddress SAD.

**Table 2** Third byte after module address MAD and subaddress SAD

FUNCTION		MSB				LSB			
		7	6	5	4	3	2	1	0
Volume left	VL	1	1	V05	V04	V03	V02	V01	V00
Volume right	VR	1	1	V15	V14	V13	V12	V11	V10
Bass	BA	1	1	1	1	BA3	BA2	BA1	BA0
Treble	TR	1	1	1	1	TR3	TR2	TR1	TR0
		1	1	1	1	1	1	1	1
		1	1	1	1	1	1	1	1
		1	1	1	1	1	1	1	1
		1	1	1	1	1	1	1	1
Switch functions	S1	1	1	MU	EFL	STL	ML1	ML0	1

**Truth tables**

Tables 3, 4 and 5 are truth tables for the switch functions

**Table 3** Mode selector

FUNCTION	ML1	ML0	IS
Stereo	1	1	1 <sup>(1)</sup>
Sound A	0	1	1 <sup>(1)</sup>
Sound B	1	0	1 <sup>(1)</sup>

**Note**

- 1. Must be set to logic 1

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**Table 4** Stereo/spatial stereo/forced mono

CHOICE	STL	EFL
Spatial stereo	1	1
Stereo	1	0
Forbidden status	0	1
Forced mono	0	0

**Table 5** Mute (see note 1)

MUTE	MU
Active; automatic after POR	1
Not active	0

**Note**

1. POR = Power-on reset.

Tables 6, 7 and 8 are truth tables for the volume, bass and treble controls

**Table 6** Volume control

2 dB/STEP (dB)	V × 5	V × 4	V × 3	V × 2	V × 1	V × 0
6	1	1	1	1	1	1
4	1	1	1	1	1	0
2	1	1	1	1	0	1
0	1	1	1	1	0	0
-2	1	1	1	0	1	1
-4	1	1	1	0	1	0
-6	1	1	1	0	0	1
-8	1	1	1	0	0	0
-10	1	1	0	1	1	1
-20	1	1	0	0	1	0
-30	1	0	1	1	0	1
-40	1	0	1	0	0	0
-50	1	0	0	0	1	1
-60	0	1	1	1	1	0
-62	0	1	1	1	0	1
-64	0	1	1	1	0	0
-80	0	1	1	0	1	1

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**Table 7** Bass control

3 dB/STEP (dB)	BA3	BA2	BA1	BA0
15	1	0	1	1
12	1	0	1	0
9	1	0	0	1
6	1	0	0	0
3	0	1	1	1
0	0	1	1	0
-3	0	1	0	1
-6	0	1	0	0
-9	0	0	1	1
-12	0	0	1	0

**Table 8** Treble control

3 dB/STEP (dB)	TR3	TR2	TR1	TR0
12	1	0	1	0
9	1	0	0	1
6	1	0	0	0
3	0	1	1	1
0	0	1	1	0
-3	0	1	0	1
-6	0	1	0	0
-9	0	0	1	1
-12	0	0	1	0



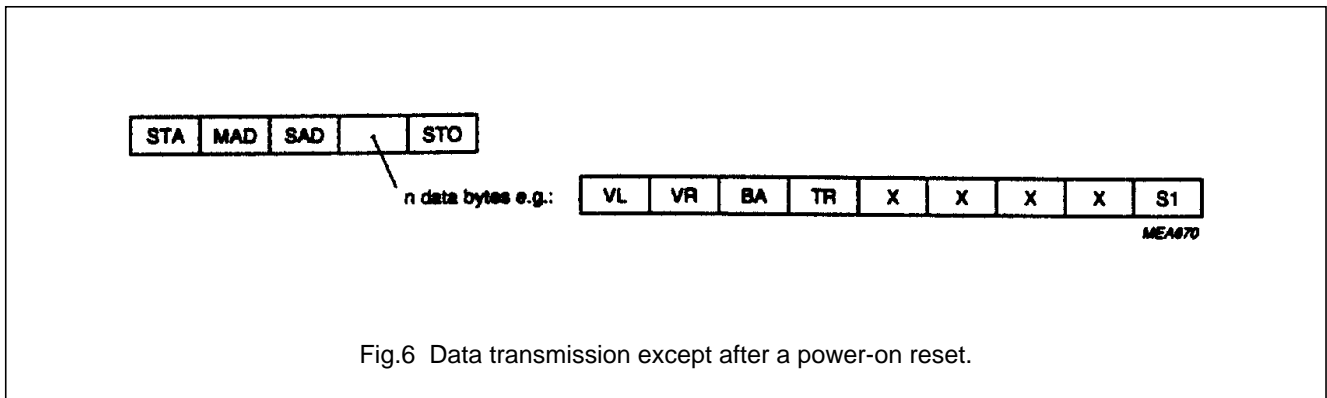
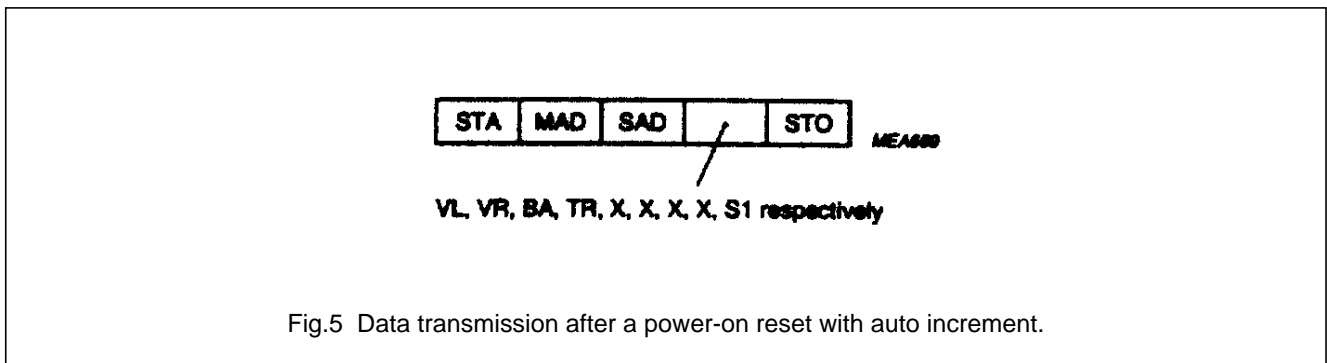
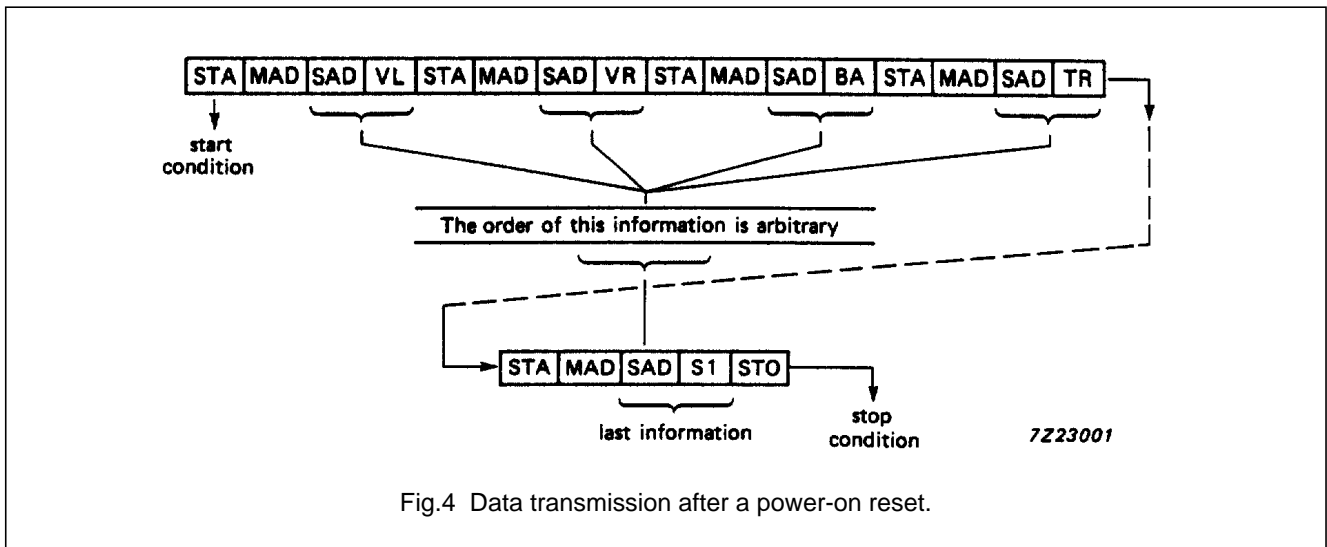
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### Sequence of data transmission

After a power-on reset all five functions have to be adjusted with five data transmissions. It is recommended that data information for switch functions are transmitted last because all functions have to be adjusted when the muting is switched off. The sequence of transmission of other data information is not critical.

The order of data transmission is shown in Figures 4 and 6. The number of data transmissions is unrestricted but before each data byte the module address MAD and the correct subaddress SAD is required.



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**LIMITING VALUES**

In accordance with Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V <sub>CC</sub>	supply voltage	0	16	V
V <sub>cap</sub>	voltage range for pins with external capacitors	0	V <sub>CC</sub>	V
V <sub>SDA, SCL</sub>	voltage range for pins 11 and 12	0	V <sub>CC</sub>	V
V <sub>I/O</sub>	voltage range at pins 1, 3, 9, 11, 12 and 13	0	V <sub>CC</sub>	V
I <sub>O</sub>	output current at pins 9 and 13	–	45	mA
P <sub>tot</sub>	total power dissipation at T <sub>amb</sub> < 70 °C	–	450	mW
T <sub>amb</sub>	operating ambient temperature range	0	+70	°C
T <sub>stg</sub>	storage temperature range	–25	+150	°C
V <sub>stat</sub>	electrostatic handling	see note 1		

**Note**

1. Electrostatic handling Human body model: C = 100 pF, R = 1.5 kΩ and V ≥ 3 kV; charge device model: C = 200 pF, R = 0 Ω and V ≥ 400 V.

**DC CHARACTERISTICS**V<sub>CC</sub> = 12 V; T<sub>amb</sub> = 25 °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Supplies</b>						
V <sub>CC</sub>	supply voltage range		10.8	12.0	13.2	V
I <sub>CC</sub>	supply current	at V <sub>CC</sub> = 12 V	–	26	35	mA
V <sub>ref</sub>	internal reference voltage		5.4	0.5V <sub>CC</sub>	6.6	V
V <sub>I</sub>	internal voltage at pins 1 and 3	DC voltage internally generated; capacitive coupling recommended	–	V <sub>ref</sub>	–	V
V <sub>O</sub>	internal voltage at pins 9 and 13		–	V <sub>ref</sub>	–	V
<b>SDA; SCL (pins 11 and 12)</b>						
V <sub>IH</sub>	HIGH level input voltage		3.0	–	V <sub>CC</sub>	V
V <sub>IL</sub>	LOW level input voltage		–3.0	–	1.5	V
I <sub>IH</sub>	HIGH level input current		–	–	+10	μA
I <sub>IL</sub>	LOW level input current		–10	–	–	μA
V <sub>cap.n</sub>	output voltage at pins with external capacitors pins 6 to 8, 14 to 16		–	V <sub>ref</sub>	–	V
V <sub>cap.2</sub>	pin 2		–	V <sub>CC</sub> –0.3	–	V

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**AC CHARACTERISTICS**

$V_{CC} = 12\text{ V}$ ; bass/treble in linear position; stereo mode; spatial stereo off;  $R_L > 10\text{ k}\Omega$ ;  $C_L < 1000\text{ pF}$ ;  $T_{amb} = 25\text{ }^\circ\text{C}$ ; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>I<sup>2</sup>C-bus timing</b> (see Fig.7)						
SDA, SCL (PINS 11 AND 12)						
$f_{SCL}$	clock frequency range		0	–	100	kHz
$t_{HIGH}$	clock HIGH period		4	–	–	$\mu\text{s}$
$t_{LOW}$	clock LOW period		4.7	–	–	$\mu\text{s}$
$t_r$	SCL rise time		–	–	1	$\mu\text{s}$
$t_f$	SCL fall time		–	–	0.3	$\mu\text{s}$
$t_{SU;STA}$	set-up time for start condition		4.7	–	–	$\mu\text{s}$
$t_{HD;STA}$	hold time for start condition		4	–	–	$\mu\text{s}$
$t_{SU;STO}$	set-up time for stop condition		4.7	–	–	$\mu\text{s}$
$t_{BUF}$	time bus must be free before a new transmission can start		4.7	–	–	$\mu\text{s}$
$t_{SU;DAT}$	data set-up time		250	–	–	ns
<b>Inputs</b>						
IN L (PIN 1) IN R (PIN 3)						
$V_{i(RMS)}$	input signal handling (RMS value)	at $V_u = -12\text{ dB}$ ; THD $\leq 0.5\%$	2	–	–	V
$R_i$	input resistance		20	30	40	$\text{k}\Omega$
f	frequency response (0.5 dB)		20	–	20 000	Hz
<b>Outputs</b>						
OUT R (PIN 9) OUT L (PIN 13)						
$V_{o(RMS)}$	output voltage range (RMS value)	at $V_{i(max)} \leq 2\text{ V}$ ; THD $\leq 0.7\%$	0.6	–	–	V
$R_L$	load resistance		10	–	–	$\text{k}\Omega$
$Z_O$	output impedance		–	–	100	$\Omega$
(S+N)/N	signal plus noise-to-noise ratio	weighted in accordance with CCIR 468-2; $V_o = 600\text{ mV}$				
	gain = 6 dB		–	78	–	dB
	gain = 0 dB		–	86	–	dB
	gain $\leq -20\text{ dB}$		–	68	–	dB
THD	total harmonic distortion	f = 20 Hz to 12.5 kHz				
	gain = +6 dB to –40 dB	$V_{i(RMS)} = 0.3\text{ V}$	–	0.05	–	%
	gain = 0 dB to –40 dB	$V_{i(RMS)} = 0.6\text{ V}$	–	0.07	0.4	%
	gain = –12 dB to –40 dB	$V_{i(RMS)} = 2.0\text{ V}$	–	0.1	–	%

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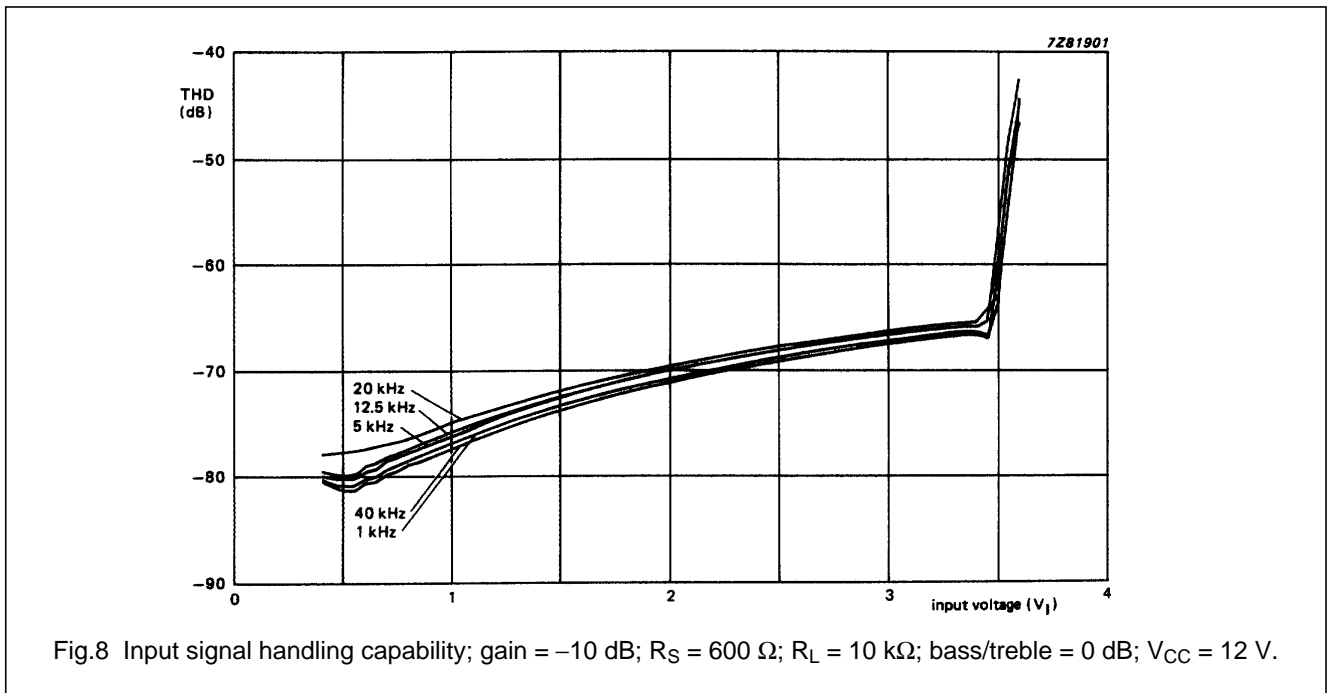
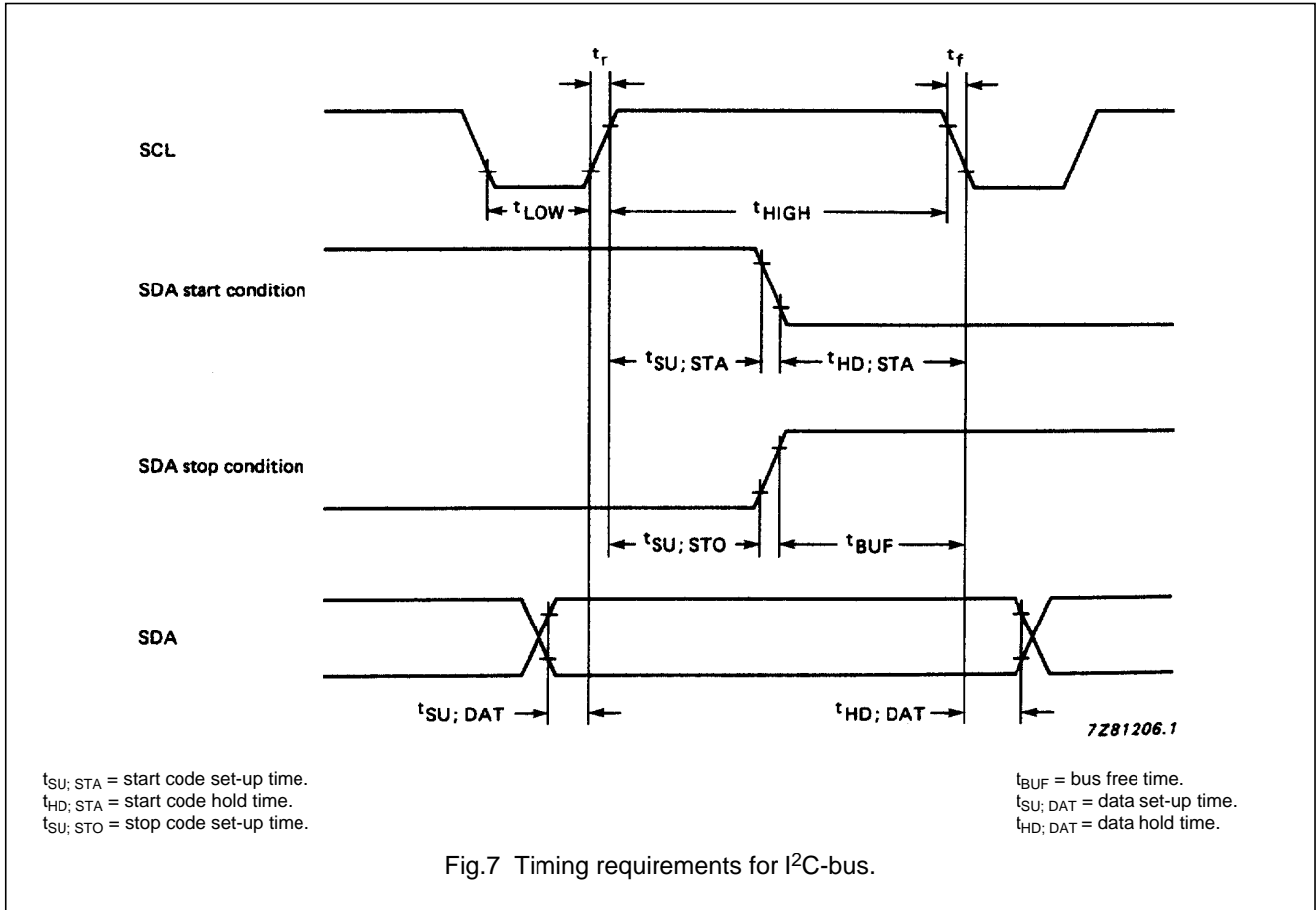
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Outputs</b>						
$\alpha_{CS}$	channel separation at 10 kHz	gain = 0 dB	–	80	–	dB
RR <sub>100</sub>	ripple rejection	$f_{ripple} = 100$ Hz; $V_{r(RMS)} < 200$ mV gain = 0 dB	–	50	–	dB
$\alpha_L$	crosstalk attenuation from logic inputs to AF outputs	gain = 0 dB	–	100	–	dB
<b>Volume control (see Table 6)</b>						
$G_{max}$	control range (36 steps) maximum voltage gain	$f = 1$ kHz 6 dB step	5	6	–	dB
$G_{min}$	minimum voltage gain	–64 dB step	–63	–64	–	dB
$G_{mute}$	mute position		–80	–90	–	dB
$G_{err}$	gain tracking error; balance in mid-position		–	–	2	dB
$G_{step}$	step resolution gain from +6 dB to –40 dB gain from –42 dB to –64 dB		1.5 1.0	2.0 2.0	2.5 3.0	dB/step dB/step
<b>Treble control (see Table 8)</b>						
$G_{emp}$	control range maximum emphasis at 15 kHz with respect to linear position	$C_{8-5}; C_{14-5} = 5.6$ nF	11	12	13	dB
$G_{att}$	maximum attenuation at 15 kHz with respect to linear position		11	12	13	dB
$G_{step}$	resolution		2.5	3.0	3.5	dB/step
<b>Bass control (see Table 7)</b>						
$G_{emp}$	control range maximum emphasis at 40 Hz with respect to linear position	$C_{6-7}; C_{15-16} = 33$ nF	14	15	16	dB
$G_{att}$	maximum attenuation at 40Hz with respect to linear position		11	12	13	dB
$G_{step}$	resolution		2.5	3.0	3.5	dB/step
<b>Spatial function</b>						
$\alpha$	antiphase crosstalk		–	52	–	%

**Note to the characteristics**

- Balance is obtained via software by different volume settings in both channels (left and right).

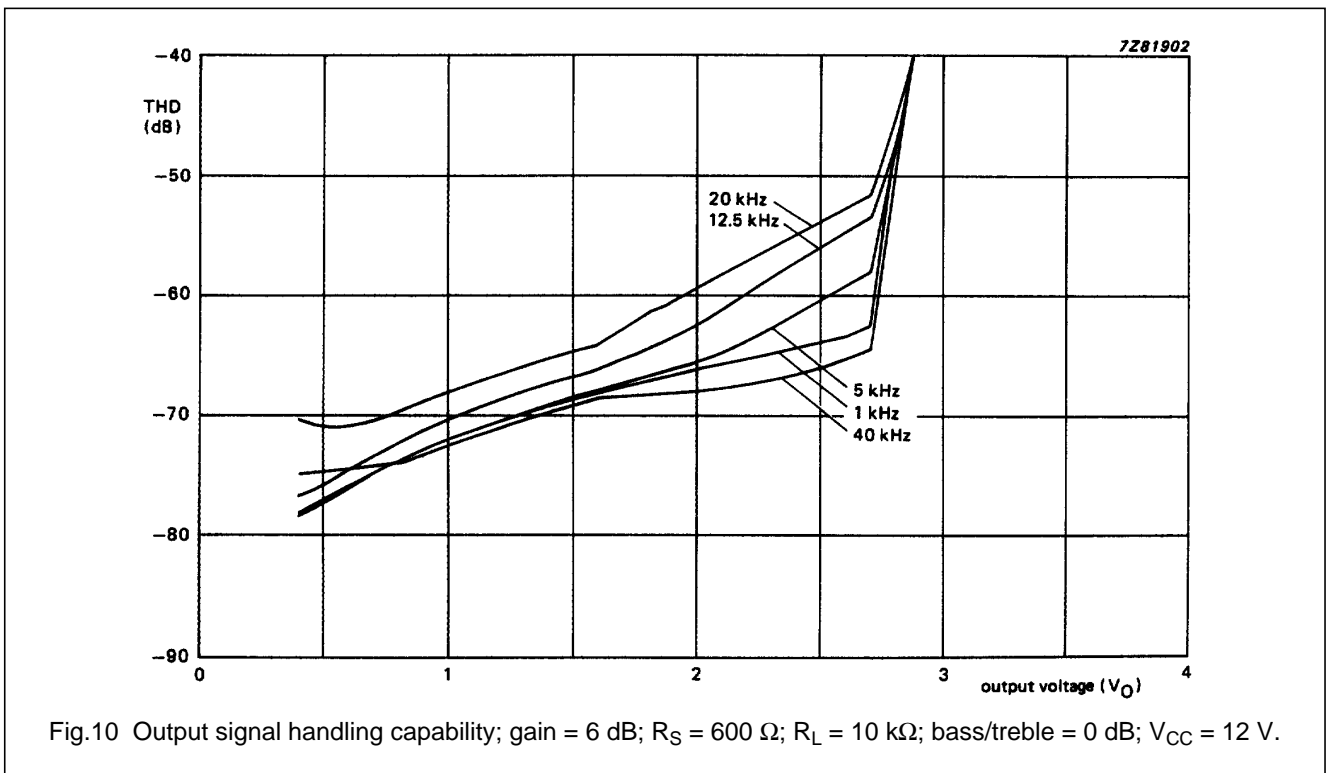
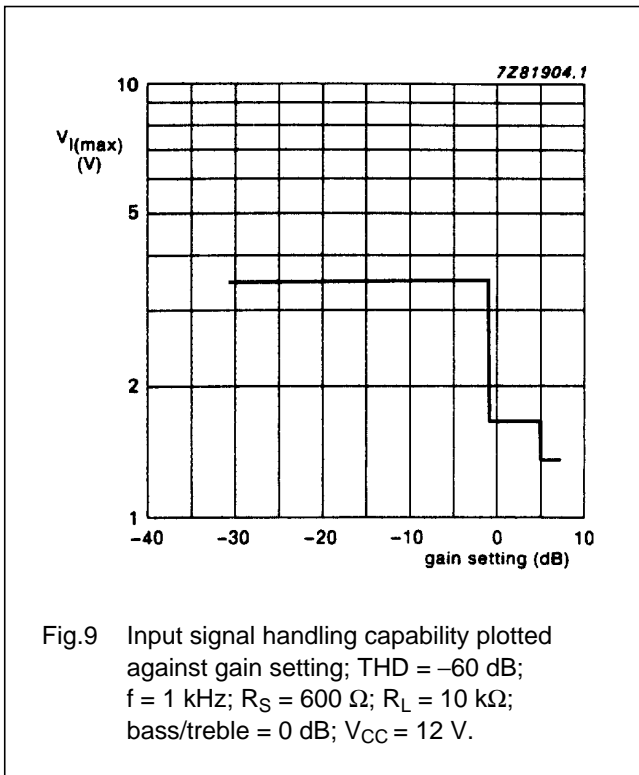
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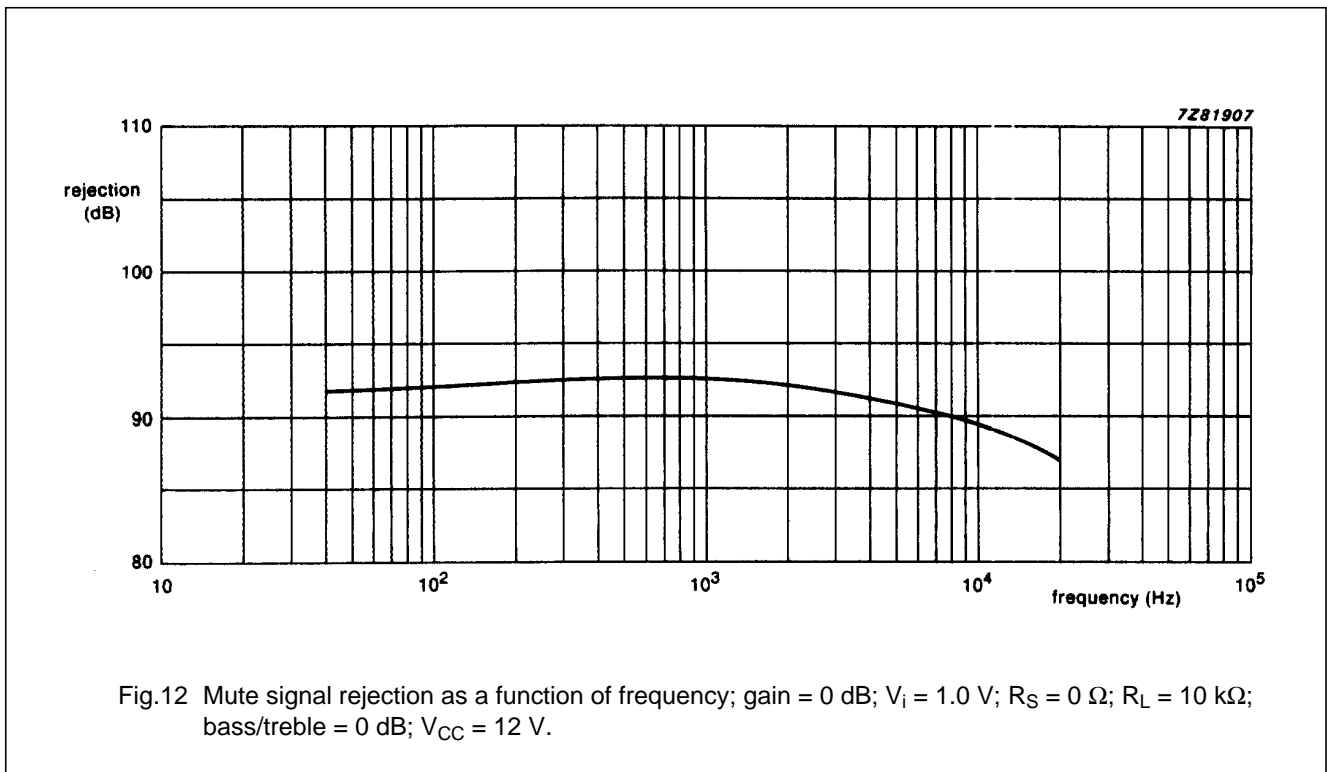
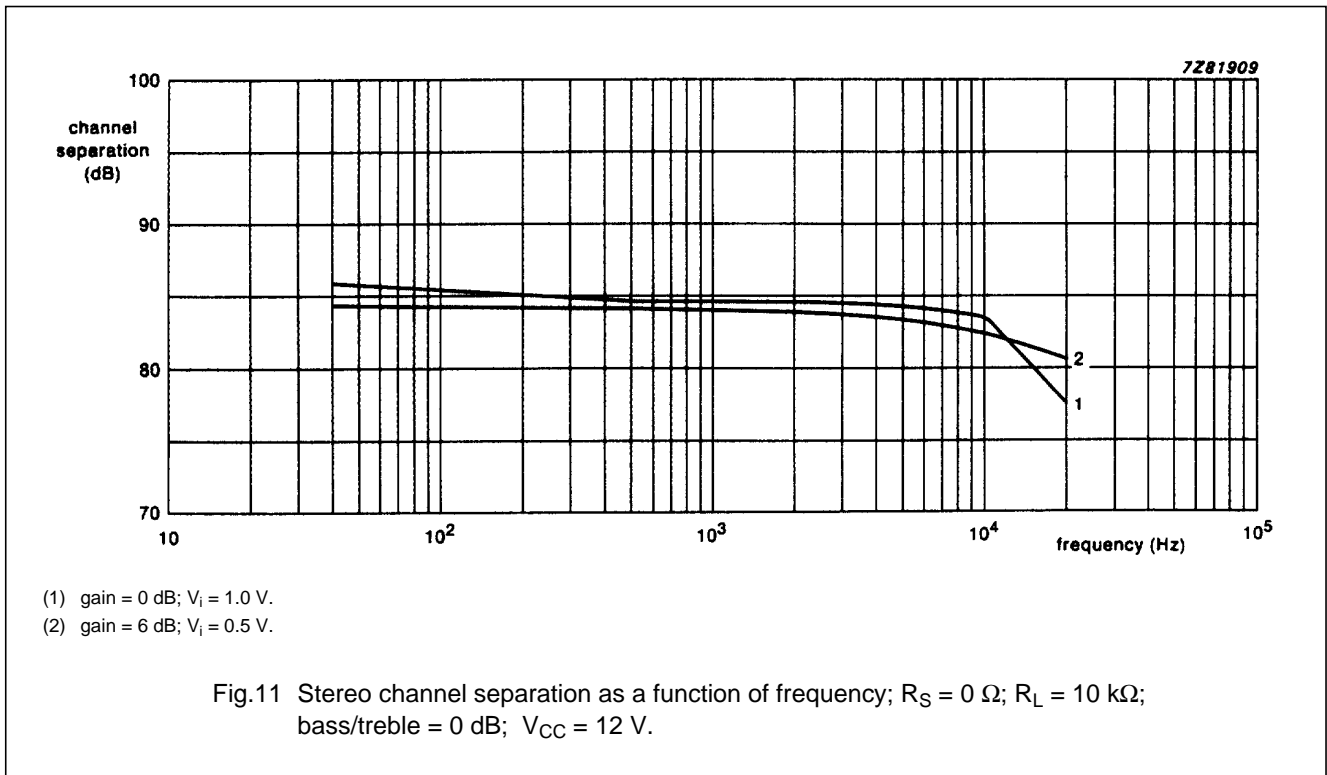
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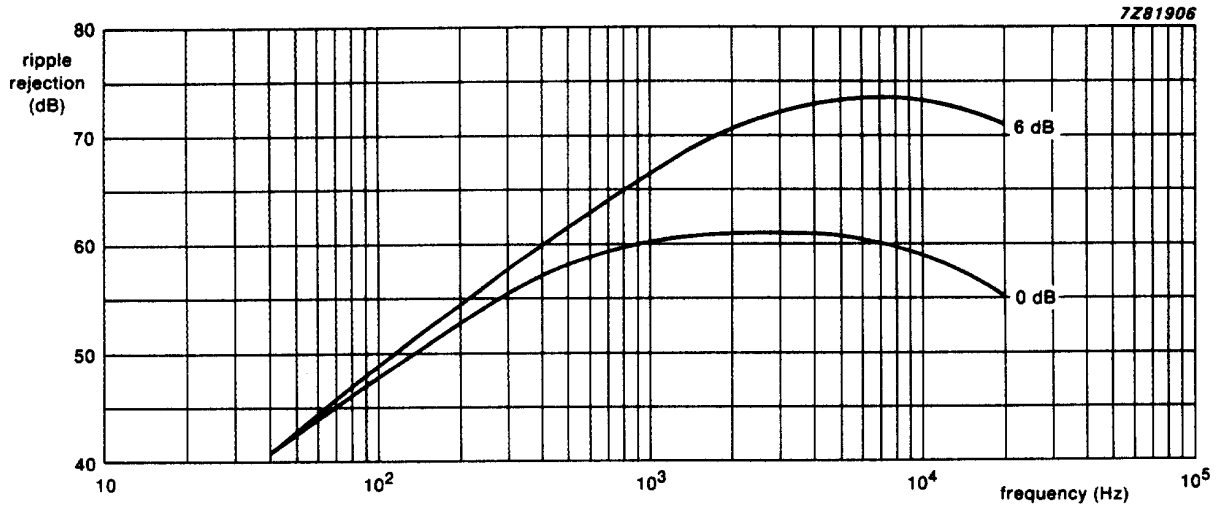


Fig.13 Ripple rejection as a function of frequency;  $V_{\text{ripple}} = 0.3 \text{ V (RMS)}$ ;  $R_S = 0 \Omega$ ;  $R_L = 10 \text{ k}\Omega$ ; bass/treble = 0 dB;  $V_{CC} = 12 \text{ V}$ .

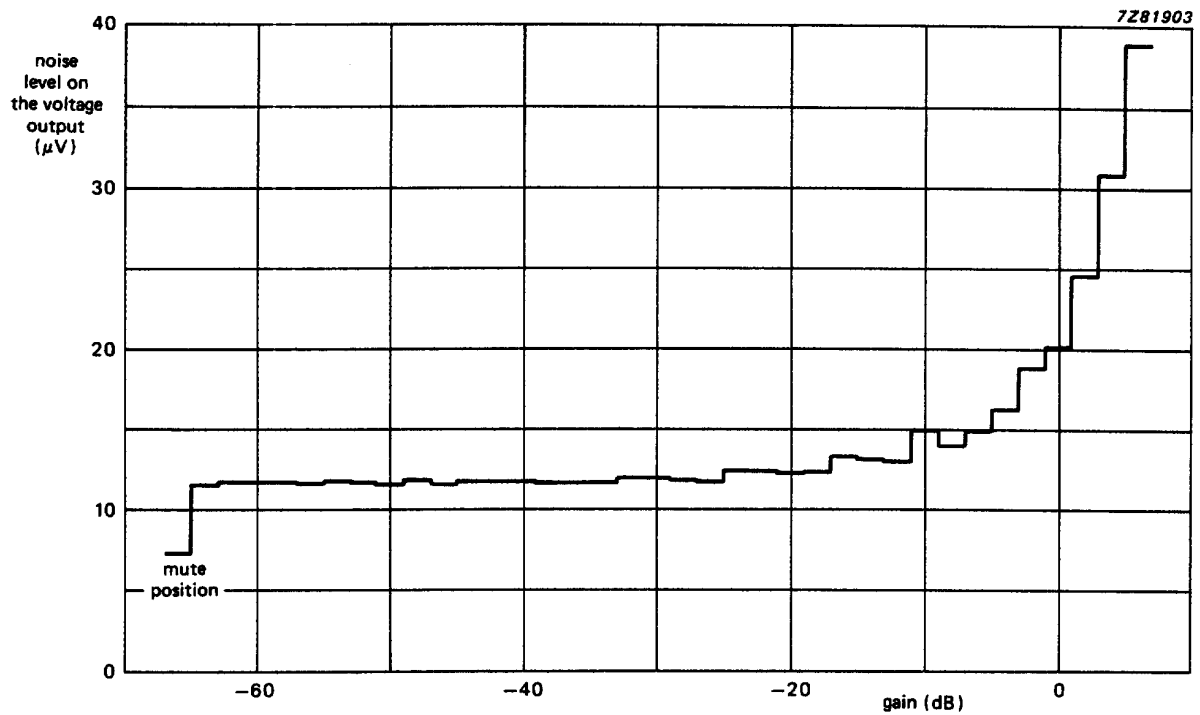


Fig.14 Noise output voltage as a function of gain; weighted CCIR 468 quasi peak gain, +6 dB to -64 dB;  $V_i = 0 \text{ V}$ ;  $R_S = 0 \Omega$ ;  $R_L = 10 \text{ k}\Omega$ ; bass/treble = 0 dB;  $V_{CC} = 12 \text{ V}$ .



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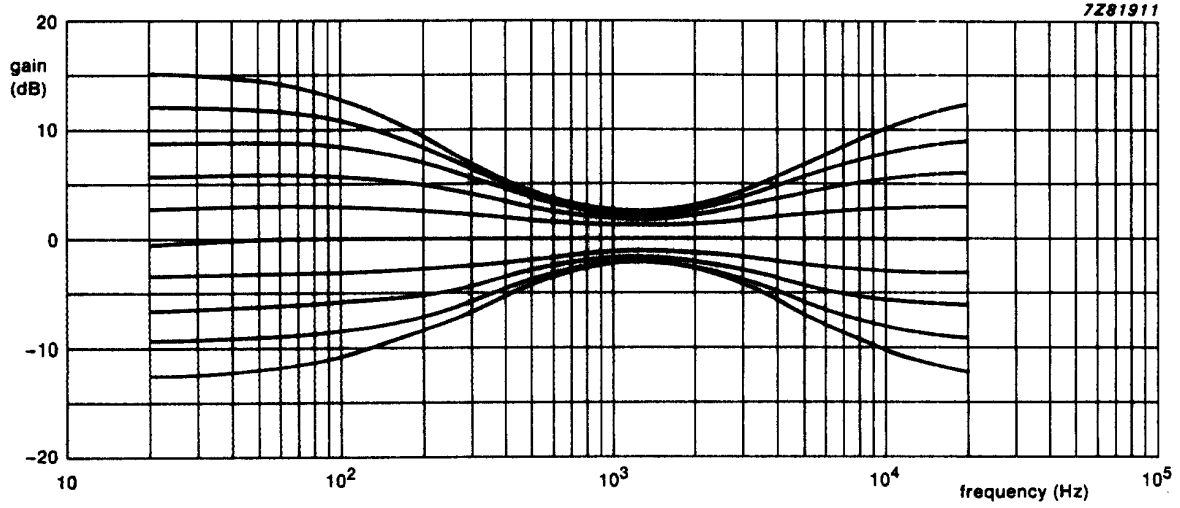


Fig.15 Frequency response of bass and treble control; bass and treble gain settings = -12 dB to +15 dB; gain = 0 dB;  $V_i = 0.1$  V;  $R_S = 600 \Omega$ ;  $R_L = 10$  k $\Omega$ ;  $V_{CC} = 12$  V.

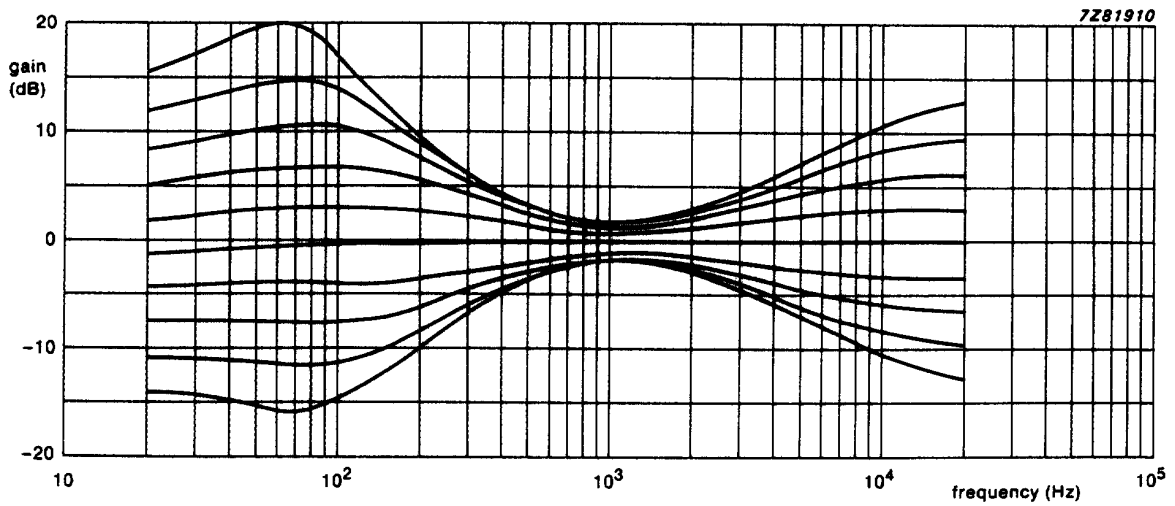
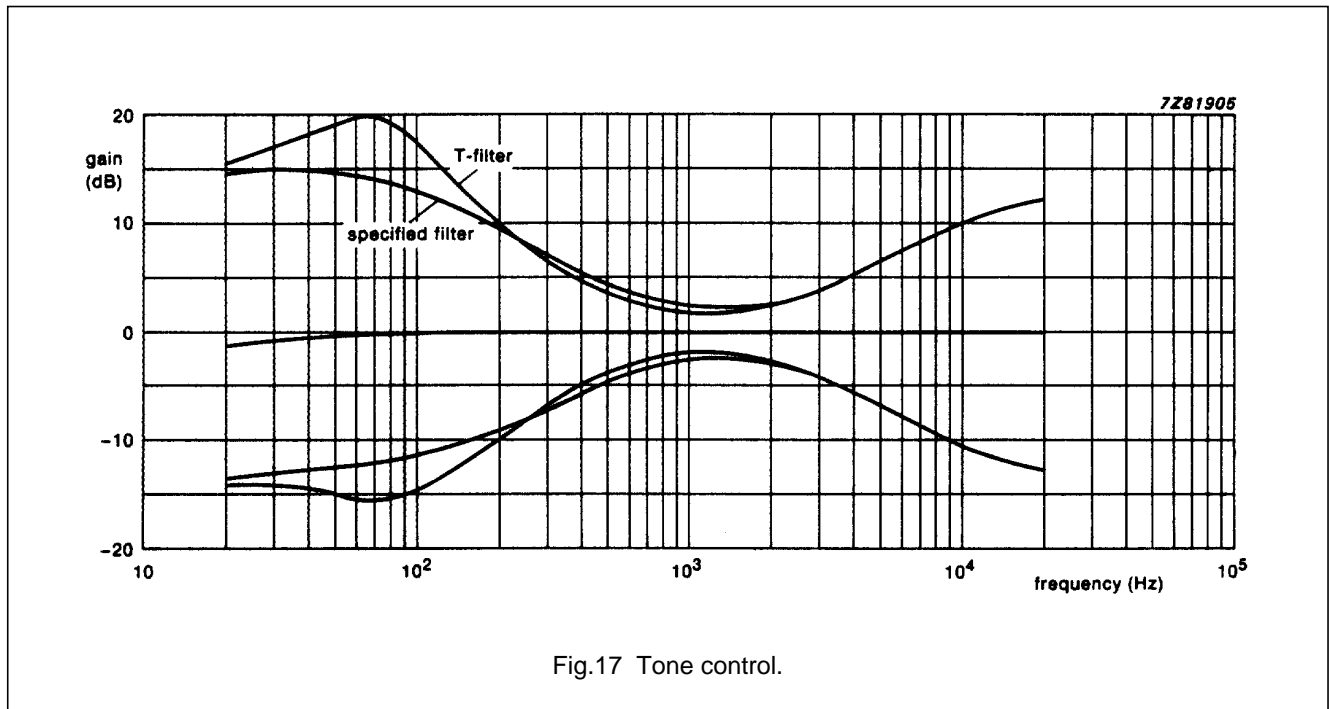


Fig.16 Tone control with T-filter.

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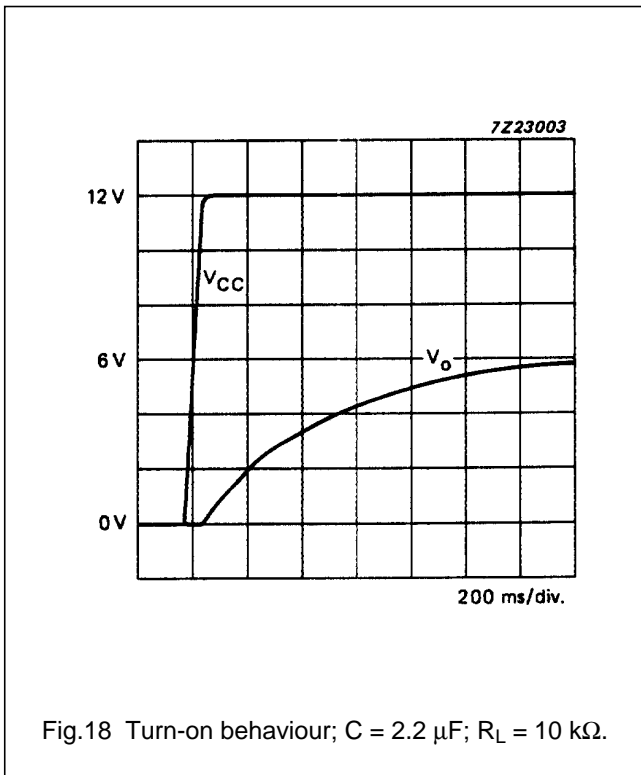


Fig.18 Turn-on behaviour;  $C = 2.2 \mu\text{F}$ ;  $R_L = 10 \text{ k}\Omega$ .

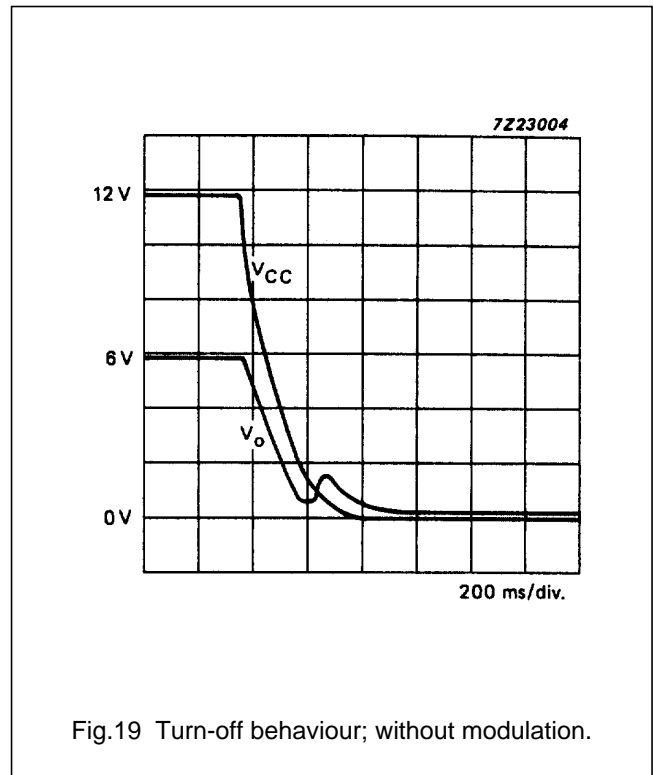


Fig.19 Turn-off behaviour; without modulation.

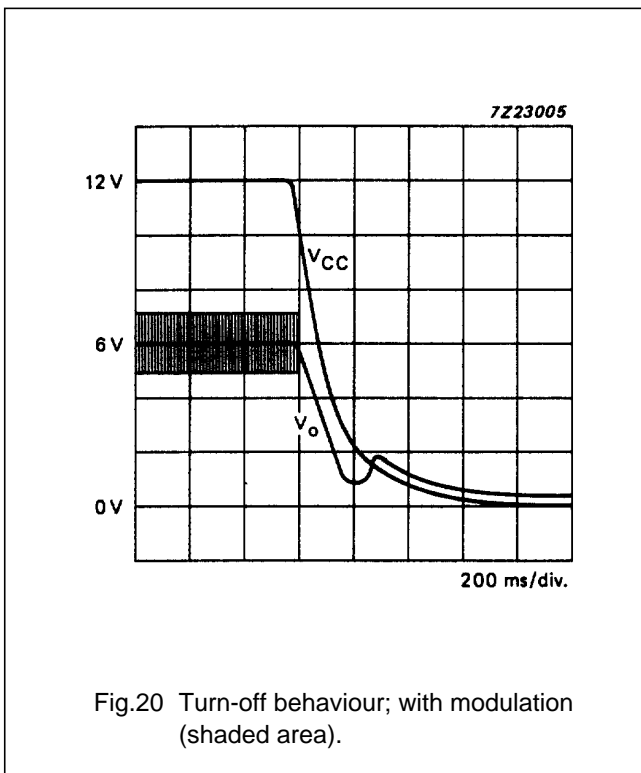
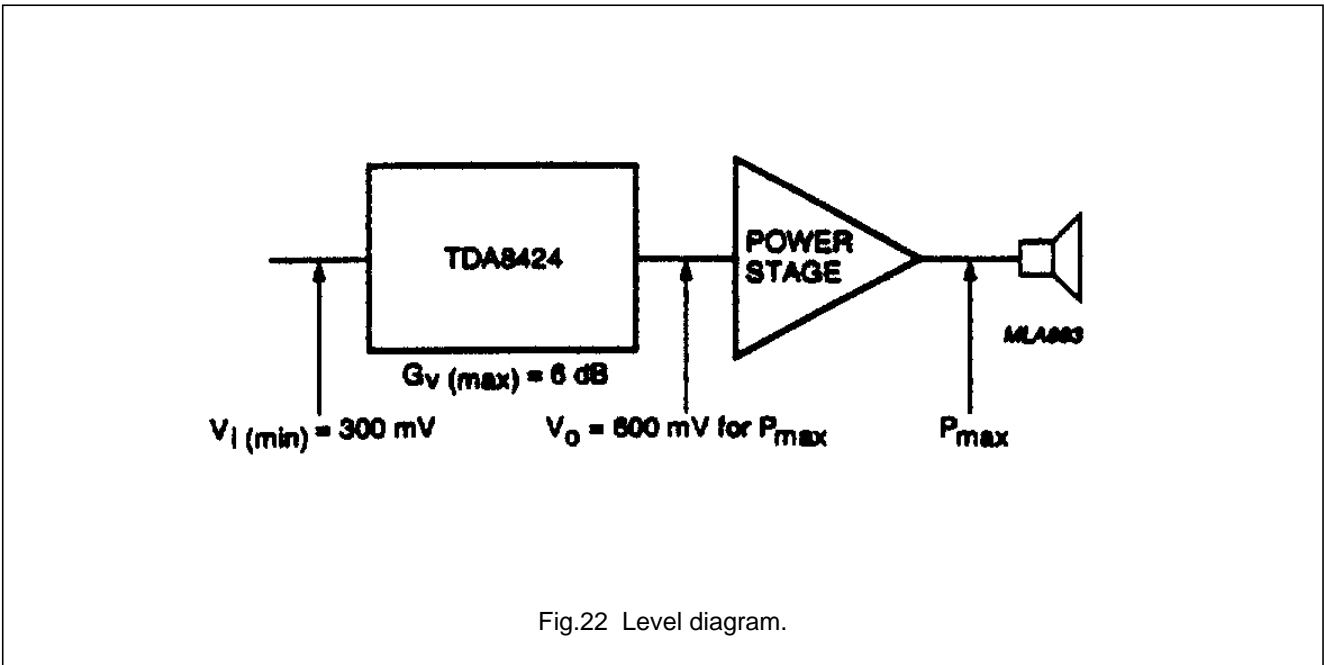
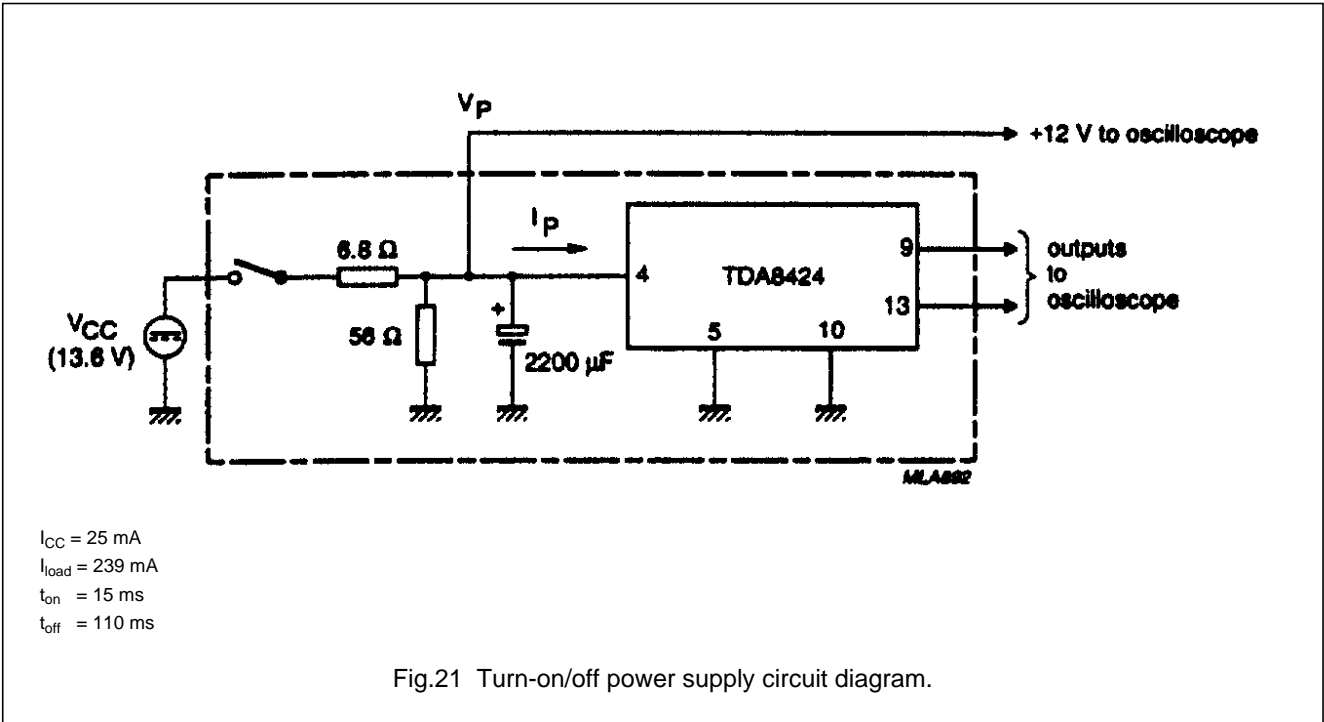


Fig.20 Turn-off behaviour; with modulation (shaded area).

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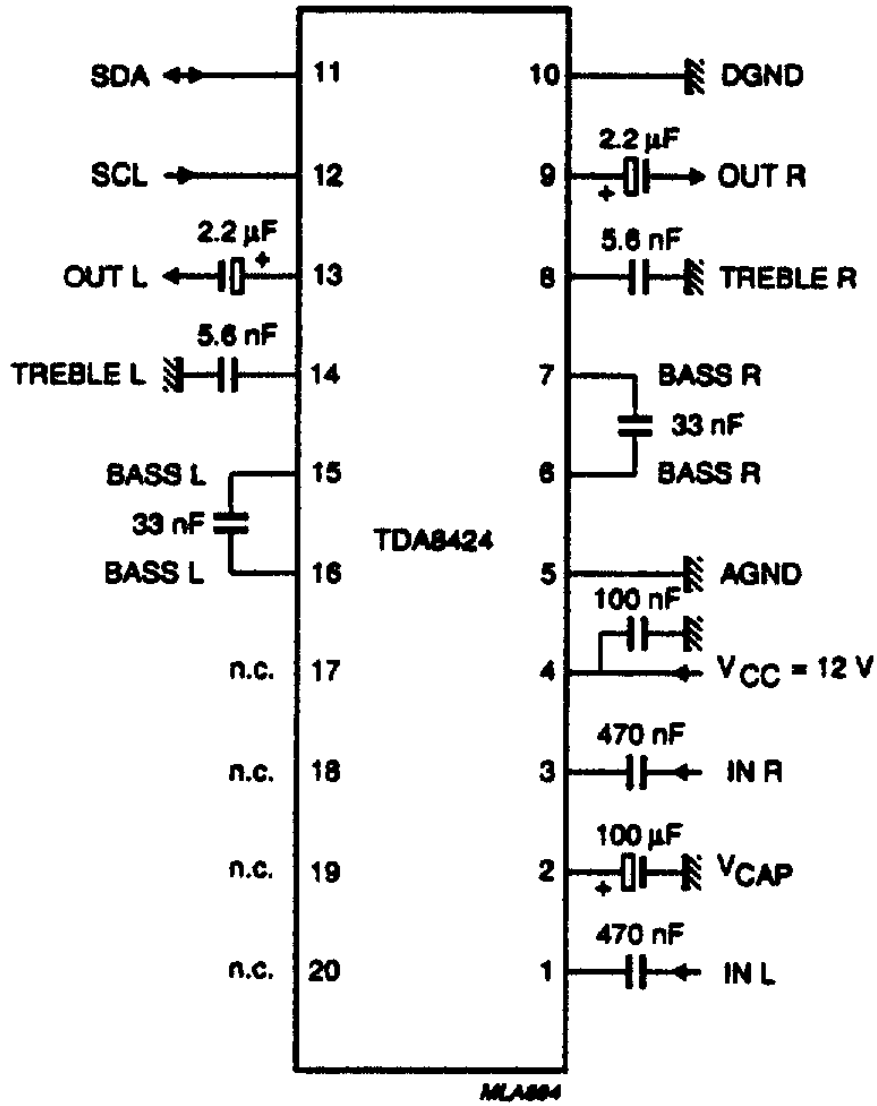


Fig.23 Test and application circuit diagram.

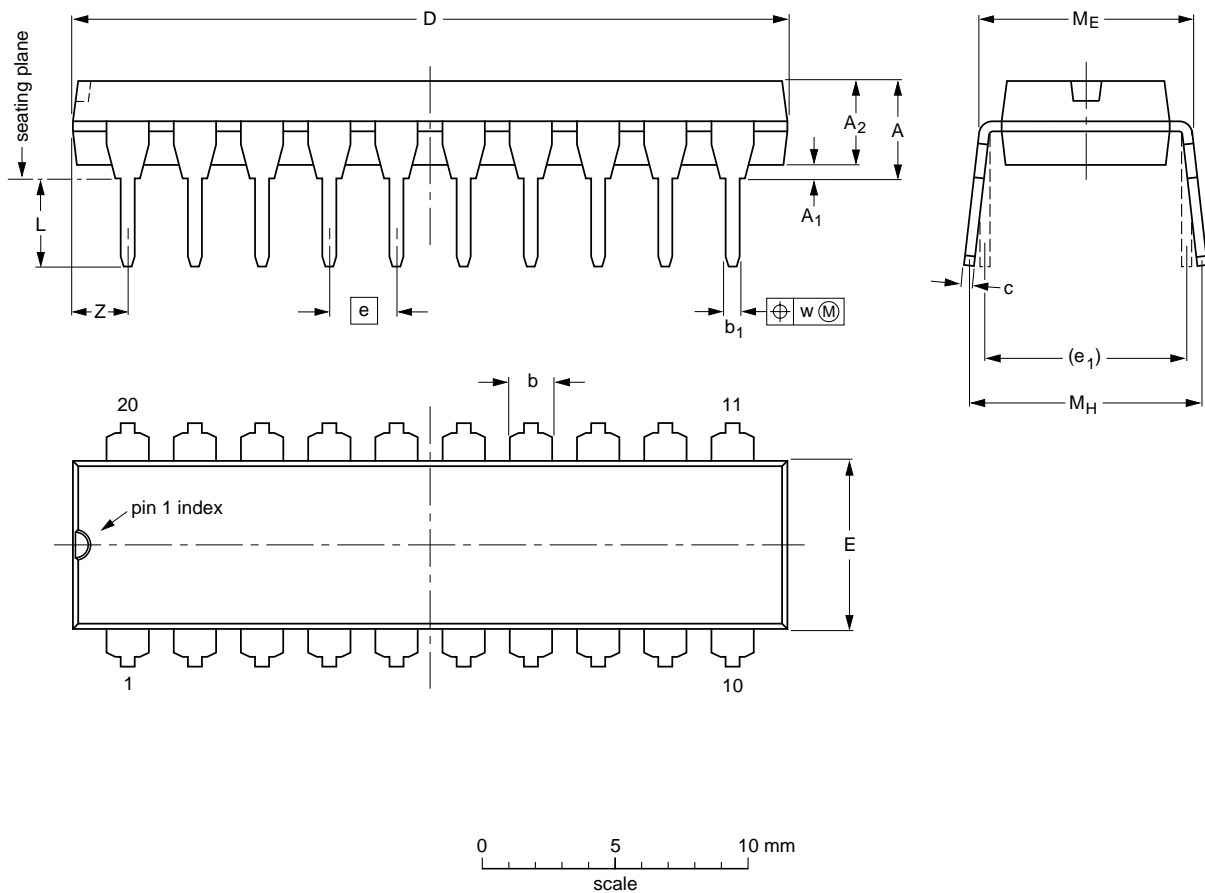
Hi-Fi stereo audio processor; I<sup>2</sup>C-bus

TDA8424

PACKAGE OUTLINE

DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			92-11-17 95-05-24

Hi-Fi stereo audio processor; I<sup>2</sup>C-bus

TDA8424

**SOLDERING****Introduction**

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our "IC Package Databook" (order code 9398 652 90011).

**Soldering by dipping or by wave**

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact

with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ( $T_{stg\ max}$ ). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

**Repairing soldered joints**

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

**DEFINITIONS**

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

**LIFE SUPPORT APPLICATIONS**

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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