

## DM74LS670 3-STATE 4-by-4 Register File

### General Description

These register files are organized as 4 words of 4 bits each, and separate on-chip decoding is provided for addressing the four word locations to either write-in or retrieve data. This permits writing into one location, and reading from another word location, simultaneously.

Four data inputs are available to supply the word to be stored. Location of the word is determined by the write select inputs A and B, in conjunction with a write-enable signal. Data applied at the inputs should be in its true form. That is, if a high level signal is desired from the output, a high level is applied at the data input for that particular bit location. The latch inputs are arranged so that new data will be accepted only if both internal address gate inputs are HIGH. When this condition exists, data at the D input is transferred to the latch output. When the write-enable input,  $G_W$ , is HIGH, the data inputs are inhibited and their levels can cause no change in the information stored in the internal latches. When the read-enable input,  $G_R$ , is HIGH, the data outputs are inhibited and go into the high impedance state.

The individual address lines permit direct acquisition of data stored in any four of the latches. Four individual decoding gates are used to complete the address for reading a word. When the read address is made in conjunction with the read-enable signal, the word appears at the four outputs.

This arrangement—data entry addressing separate from data read addressing and individual sense line — elimi-

nates recovery times, permits simultaneous reading and writing, and is limited in speed only by the write time (27 ns typical) and the read time (24 ns typical). The register file has a non-volatile readout in that data is not lost when addressed.

All inputs (except read enable and write enable) are buffered to lower the drive requirements to one normal Series DM74LS load, and input clamping diodes minimize switching transients to simplify system design. High speed, double ended AND-OR-INVERT gates are employed for the read-address function and have high sink current, 3-STATE outputs. Up to 128 of these outputs may be wire-AND connected for increasing the capacity up to 512 words. Any number of these registers may be paralleled to provide n-bit word length.

### Features

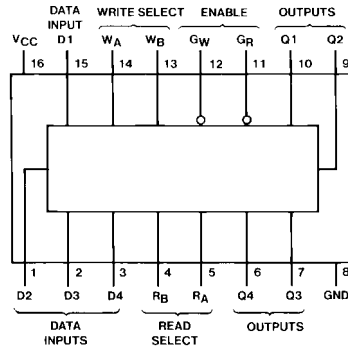
- For use as:
  - Scratch pad memory
  - Buffer storage between processors
  - Bit storage in fast multiplication designs
- Separate read/write addressing permits simultaneous reading and writing
- Organized as 4 words of 4 bits
- Expandable to 512 words of n-bits
- 3-STATE versions of DM74LS170
- Fast access times 20 ns typ

### Ordering Code:

Order Number	Package Number	Package Description
DM74LS670M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
DM74LS670N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

## Connection Diagram



## Function Tables

**Write Table** (Note 1)(Note 2)

Write Inputs			Word			
W <sub>B</sub>	W <sub>A</sub>	G <sub>W</sub>	0	1	2	3
L	L	L	Q = D	Q <sub>0</sub>	Q <sub>0</sub>	Q <sub>0</sub>
L	H	L	Q <sub>0</sub>	Q = D	Q <sub>0</sub>	Q <sub>0</sub>
H	L	L	Q <sub>0</sub>	Q <sub>0</sub>	Q = D	Q <sub>0</sub>
H	H	L	Q <sub>0</sub>	Q <sub>0</sub>	Q <sub>0</sub>	Q = D
X	X	H	Q <sub>0</sub>	Q <sub>0</sub>	Q <sub>0</sub>	Q <sub>0</sub>

**Read Table** (Note 3)

Read Inputs			Outputs			
R <sub>B</sub>	R <sub>A</sub>	G <sub>R</sub>	Q1	Q2	Q3	Q4
L	L	L	WOB1	WOB2	WOB3	WOB4
L	H	L	W1B1	W1B2	W1B3	W1B4
H	L	L	W2B1	W2B2	W2B3	W2B4
H	H	L	W3B1	W3B2	W3B3	W3B4
X	X	H	Z	Z	Z	Z

H = HIGH Level

L = LOW Level

X = Don't Care

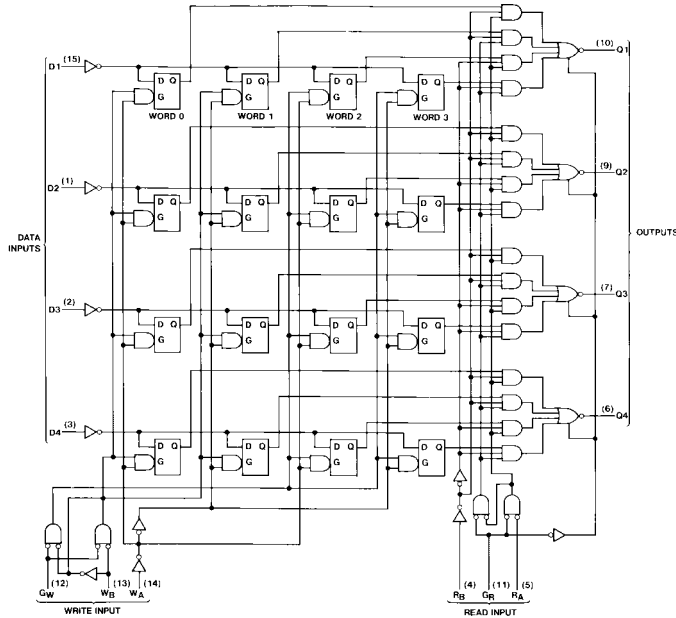
Z = High Impedance (OFF)

**Note 1:** (Q = D) = The four selected internal flip-flop outputs will assume the states applied to the four external data inputs.

**Note 2:** Q<sub>0</sub> = The level of Q before the indicated input conditions were established.

**Note 3:** WOB1 = The first bit of word 0, etc.

## Logic Diagram



**Absolute Maximum Ratings**(Note 4)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	-65°C to +150°C

**Note 4:** The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Recommended Operating Conditions**

Symbol	Parameter	Min	Nom	Max	Units
$V_{CC}$	Supply Voltage	4.75	5	5.25	V
$V_{IH}$	HIGH Level Input Voltage	2			V
$V_{IL}$	LOW Level Input Voltage			0.8	V
$I_{OH}$	HIGH Level Output Current			-2.6	mA
$I_{OL}$	LOW Level Output Current			24	mA
$t_W$	Write Enable Pulse Width (Note 5)	25			ns
$t_{SU}$	Setup Time (Note 5)(Note 6)	Data	10		ns
		$W_A, W_B$	15		
$t_H$	Hold Time (Note 5)(Note 6)	Data	15		ns
		$W_A, W_B$	5		
$t_{LATCH}$	Latch Time for New Data (Note 5)(Note 7)	25			ns
$T_A$	Free Air Operating Temperature	0		70	°C

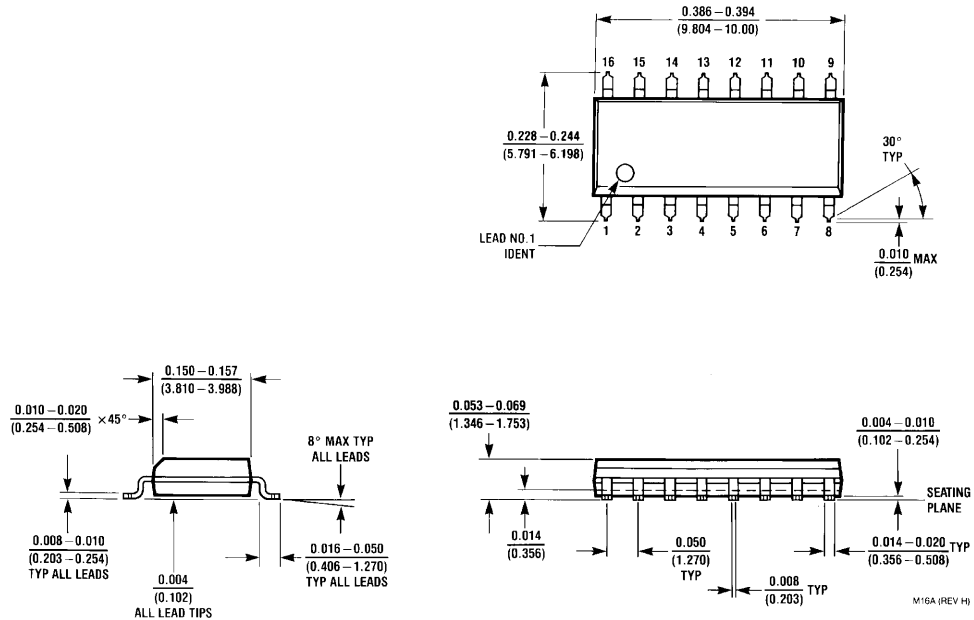
**Note 5:**  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 5\text{V}$ .

**Note 6:** Times are with respect to the Write-Enable input. Write-Select time will protect the data written into the previous address. If protection of data in the previous address,  $t_{SETUP}(W_A, W_B)$  can be ignored. As any address selection sustained for the final 30 ns of the Write-Enable pulse and during  $t_H(W_A, W_B)$  will result in data being written into that location. Depending on the duration of the input conditions, one or a number of previous addresses may have been written into.

**Note 7:** Latch time is the time allowed for the internal output of the latch to assume the state of new data. This is important only when attempting to read from a location immediately after that location has received new data.

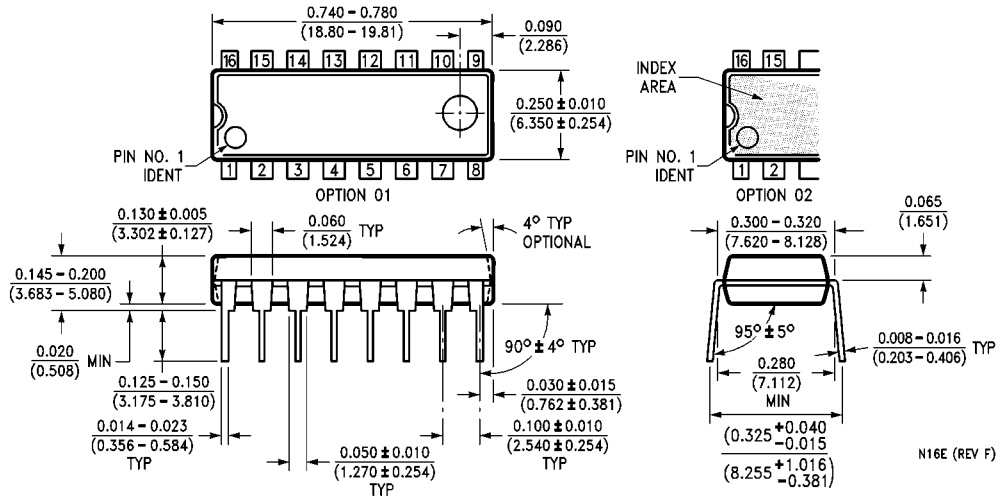
Electrical Characteristics							
over recommended operating free air temperature range (unless otherwise noted)							
Symbol	Parameter	Conditions	Min	Typ (Note 8)	Max	Units	
$V_I$	Input Clamp Voltage	$V_{CC} = \text{Min}$ , $I_I = -18 \text{ mA}$			-1.5	V	
$V_{OH}$	HIGH Level Output Voltage	$V_{CC} = \text{Min}$ , $I_{OH} = \text{Max}$ $V_{IL} = \text{Max}$ , $V_{IH} = \text{Min}$	2.4	3.4		V	
$V_{OL}$	LOW Level Output Voltage	$V_{CC} = \text{Min}$ , $I_{OL} = \text{Max}$ $I_{OL} = \text{Max}$ , $V_{IH} = \text{Min}$		0.34	0.5	V	
$I_I$	Input Current @ Max Input Voltage	$V_{CC} = \text{Max}$ $V_I = 7\text{V}$	D, R or W		0.1	mA	
			$G_W$		0.2		
			$G_R$		0.3		
$I_{IH}$	HIGH Level Input Current	$V_{CC} = \text{Max}$ $V_I = 2.7\text{V}$	D, R or W		20	$\mu\text{A}$	
			$G_W$		40		
			$G_R$		60		
$I_{IL}$	LOW Level Input Current	$V_{CC} = \text{Max}$ $V_I = 0.4\text{V}$	D, R or W		-0.4	mA	
			$G_W$		-0.8		
			$G_R$		-1.2		
$I_{OZH}$	Off-State Output Current with HIGH Level Output Voltage Applied	$V_{CC} = \text{Max}$ , $V_O = 2.7\text{V}$ $V_{IH} = \text{Min}$ , $V_{IL} = \text{Max}$			20	$\mu\text{A}$	
$I_{OZL}$	Off-State Output Current with LOW Level Output Voltage Applied	$V_{CC} = \text{Max}$ , $V_O = 0.4\text{V}$ $V_{IH} = \text{Min}$ , $V_{IL} = \text{Max}$			-20	$\mu\text{A}$	
$I_{OS}$	Short Circuit Output Current	$V_{CC} = \text{Max}$ (Note 9)	-20		-100	mA	
$I_{CC}$	Supply Current	$V_{CC} = \text{Max}$ (Note 10)		30	50	mA	
<b>Note 8:</b> All typicals are at $V_{CC} = 5\text{V}$ , $T_A = 25^\circ\text{C}$ .							
<b>Note 9:</b> Not more than one output should be shorted at a time, and the duration should not exceed one second.							
<b>Note 10:</b> $I_{CC}$ is measured with 4.5V applied to all DATA inputs and both ENABLE inputs, all ADDRESS inputs are grounded and all outputs are OPEN.							
Switching Characteristics							
at $V_{CC} = 5\text{V}$ and $T_A = 25^\circ\text{C}$							
Symbol	Parameter	From (Input) To (Output)	$R_L = 667\Omega$				Units
			$C_L = 45 \text{ pF}$		$C_L = 150 \text{ pF}$		
			Min	Max	Min	Max	
$t_{PLH}$	Propagation Delay Time LOW-to-HIGH Level Output	Read Select to Q		40		50	ns
$t_{PHL}$	Propagation Delay Time HIGH-to-LOW Level Output	Read Select to Q		45		55	ns
$t_{PLH}$	Propagation Delay Time LOW-to-HIGH Level Output	Write Enable to Q		45		55	ns
$t_{PHL}$	Propagation Delay Time HIGH-to-LOW Level Output	Write Enable to Q		50		60	ns
$t_{PLH}$	Propagation Delay Time LOW-to-HIGH Level Output	Data to Q		45		55	ns
$t_{PHL}$	Propagation Delay Time HIGH-to-LOW Level Output	Data to Q		40		50	ns
$t_{PZH}$	Output Enable Time to HIGH Level Output	Read Enable to Any Q		35		45	ns
$t_{PZL}$	Output Enable Time to LOW Level Output	Read Enable to Any Q		40		50	ns
$t_{PHZ}$	Output Disable Time from HIGH Level Output (Note 11)	Read Enable to Any Q		50			ns
$t_{PLZ}$	Output Disable Time from LOW Level Output (Note 11)	Read Enable to Any Q		35			ns
<b>Note 11:</b> $C_L = 5 \text{ pF}$ .							

**Physical Dimensions** inches (millimeters) unless otherwise noted



**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow Package Number M16A**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N16E**

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