a module solution provider

WG1300-B0 WLAN Module

TI CC3000 IEEE 802.11b/g solution

Datasheet

Draft 0.2

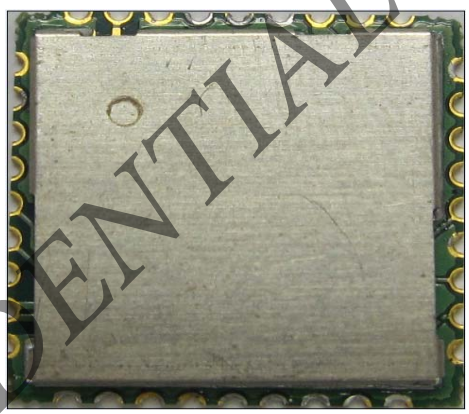
FEATURES

- IEEE 802.11 b/g compliant.
- Compact footprint: 14.5mmx14.5mmx2mm
- Operating Voltage: 2.9~4.8V
- Operating temperature: -40~85℃
- Embedded Wi-Fi and networking software

  Including drivers, stack, and supplicant
  - ➢ Universal IP connectivity enabled anywhere
  - ➢ Pair easily with low-memory, low-cost, Low-power microcontroller systems
  - ➢ Implement Wi-Fi quickly without previous Wi-Fi or RF experience
- Credible, proven solution with best-in-class Budget
  - ➢ Long range, reliable coverage throughout the entire house
  - ➢ Proven Wi-Fi interoperability
- Complete platform solution and certified modules
  - ➢ Get started quickly with sample applications on multiple platforms
  - ➢ Comprehensive documentation and support community
  - ➢ Porting documentation available to allow MCU flexibility

DESCRIPTION

WG1300-B0 is a 2.4GHz WLAN module which can be integrated with any low-cost/low power MCU to makes it the ideal solution for embedded applications.



With the necessary PHY, MAC and network layers, it makes WG1300-B0 can support WLAN application via SPI bus to communicate with host microcontrollers or other embedded processors.

With worldwide certificates, customers can leverage modular certificate by adopting the same antenna and RF trace routing to save development cost and speed up time to market by following its reference design.

APPLICATIONS

- Home entertainment control
- Thermostats, appliances
- HVAC controller, remote displays
- Home Network aggregators
- Remote appliance diagnostics/support
- Remote storage devices
- Cameras and video surveillance
- Toys
- Gaming

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1. FUNCTIONAL FEATURES

1.1. Module Block Diagram

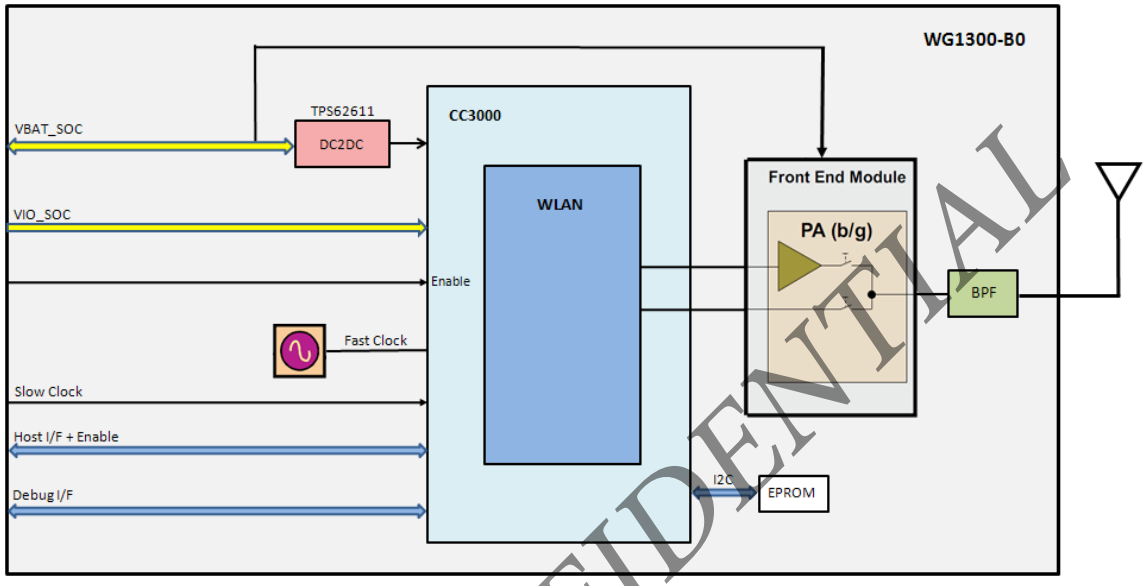


Figure 1 Module Block Diagram

1.2. Functional Block Feature

1.2.1. WLAN Features

WLAN MAC Baseband Processor and RF transceiver which is IEEE802.11b/g compliant

- Accepts 26MHz reference clock Input
- IEEE Std 802.11d,i PICS compliant
- Supports Serial Peripheral Interface (SPI) Host Interface
- Medium-Access Controller (MAC)
  - Embedded ARM™ Central Processing Unit (CPU)
  - Hardware-Based Encryption/Decryption Using 64-, 128-Bit WEP, TKIP or AES Keys
  - Supports requirements for Wireless Fidelity (Wi-Fi) Protected Access (WPA and WPA2.0) and IEEE Std 802.11i [Includes Hardware-Accelerated Adanced-Encrytion Standard (AES)]

- Baseband Processor
- 2.4GHz Radio
  - Digital Radio Processor (DRP) implementation
  - Internal LNA
  - Supports : IEEE Std 802.11b, 802.11g, 802.11b/g

1.2.2. Network Stack Supported Protocols

- Transport layer
  - TCP
  - UDP
- Network layer
  - IPv4
  - Ping
  - DHCP
  - DNS Client
- Link layer
  - ARP

1.2.3. Wireless Security System Features

- Supported modes
  - Open (no security)
  - WEP
  - WPA-Personal
  - WPA2-Personal
- Supported encryption types
  - WEP
  - TKIP
  - AES
  - Open

2. MODULE SPECIFICATION

2.1. Absolute Maximum Ratings

Parameters	Min	Max	Unit
Power supply Voltage (VBAT_IN)	–0.5	+5.5 (1)	V
Voltage of digital pins (2)	–0.5	+3.6	V
Voltage of EEPROM and RS232 test signals	–0.5	2.1	V
Operating Temperature	–40	+85 (3)	°C
Storage Temperature	–55	+125	°C

(1) Maximum allowed depends on accumulated time at that voltage; 4.8V for 7 years lifetime,5.5V for 6 hours cumulative.

(2) This includes the SPI and Power Enable signals

(3) The device can be reliably operated for 5,000 active-WLAN cumulative hours at TA of 85°C.

Table 1 Absolute Maximum Ratings

2.2. Recommended Operating Conditions

Recommended Operating Conditions

Parameters	Min	TYP	Max	Unit
VBAT_IN	2.9	3.3	4.8	V
Voltage of digital pins	0	3.3	3.6	V
Voltage of EEPROM and RS232 test signals	0		1.8	V
Operating Temperature	–30	25	75	°C

Table 2 Recommended Operating Conditions

2.3. General Characteristics

DC Characteristics (RS232/EEPROM I/O)

Parameters	Test Conditions	Min	Max	Unit
Logic input low, V_{IL}	--	0	0.67	V
Logic input high, V_{IH}	--	1.05	1.92	V
Logic output low, V_{OL}	4.8mA	0	0.45	V
Logic output high, V_{OH}	4.8mA	1.17	1.92	V

Table 3 DC Characteristics General Purpose I/O

3. MODULE OUTLINE

3.1. Footprint and pinouts

For PCB layout, the footprint below is recommended for your applications.

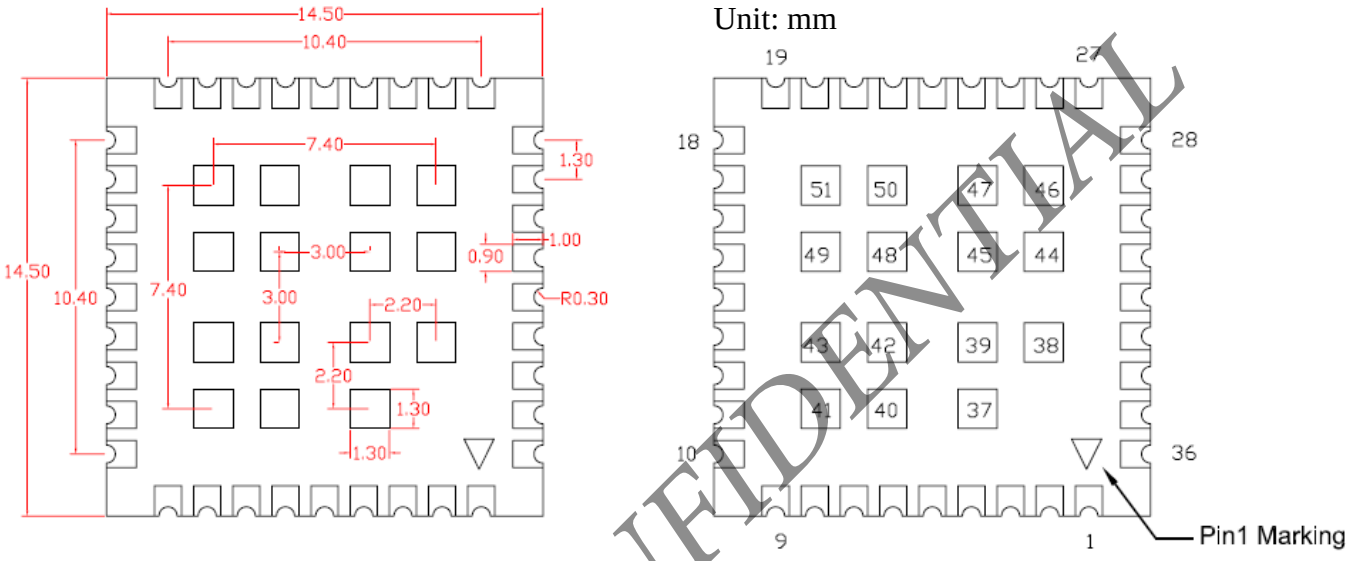


Figure 2 WG1300-B0 Footprint and Pinouts

3.2. Pin Description

Pin #	Signal Name	Type	Description
1	GND	GND	Ground
2	WL_UART_DBG	I	WL_UART_DBG
3	WL_EN2 (1)	O	WL_EN2
4	WL_EN1 (2)	O	WL_EN1.
5	WL_RS232_TX (3)	I	WL_RS232_TX (Test-mode signal, 1.8V Logic)
6	WL_RS232_RX (3)	O	WL_RS232_RX (Test-mode signal, 1.8V Logic)
7	GND	GND	Ground
8	VIO_SOC	Power	Module VIO Supply
9	GND	GND	Ground

10	GND	GND	Ground
11	SPI_DIN	I	HOST Interface SPI Data In
12	SPI_DOUT	I	HOST Interface SPI Data Out
13	SPI_IRQ	O	HOST Interface SPI Interrupt
14	SPI_CLK	O	HOST Interface SPI CLOCK
15	SPI_CS	O	HOST Interface SPI Chip Select
16	GND	GND	Ground
17	EXT_32K	CLK	EXTERNAL SLOW CLOCK FROM HOST
18	GND	GND	Ground
19	GND	GND	Ground
20	XTALP		Fref Input
21	XTALM		Fref Input
22	GND	GND	Ground
23	SCL_EEPROM (4)	I/O	I2C CLOCK LINE FROM EEPROM.
24	SCL_CC3000 (4)	I/O	I2C CLOCK LINE FROM CC3000.
25	SDA_EEPROM (5)	I/O	I2C DATA LINE FROM EEPROM.
26	SDA_CC3000 (5)	I/O	I2C DATA LINE FROM CC3000.
27	GND	GND	Ground
28	VBAT_IN	Power	Power Supply to Module
29	GND	GND	Ground
30	DC2DC_OUT	I	1.8V Supply
31	GND	GND	Ground
32	CLK_REQ_OUT	I/O	Clock request out
33	NS_UARTD	I/O	Networking subsystem; UART Debug line
34	GND	GND	Ground
35	RF_ANT	RF	WLAN ANT Port
36	GND	GND	Ground
37	GND	GND	Ground
38	GND	GND	Ground

39	GND	GND	Ground
40	GND	GND	Ground
41	GND	GND	Ground
42	GND	GND	Ground
43	GND	GND	Ground
44	GND	GND	Ground
45	GND	GND	Ground
46	GND	GND	Ground
47	GND	GND	Ground
48	GND	GND	Ground
49	GND	GND	Ground
50	GND	GND	Ground
51	GND	GND	Ground

(1) Short to WL_EN1 (Pin #7) for function mode.

(2) Short to GND for test mode; Short to WL_EN2 (Pin #5) for function mode.

(3) Left unconnected for function mode

(4) I2C Clock lines from EEPROM and CC3000 must be connected together for function mode.

(5) I2C Data lines from EEPROM and CC3000 must be connected together for function mode.

Table 4 WG1300-B0 Pin Description

4. SPI HOST CONTROLLER INTERFACE

WG1300-B0 communicates with HOST via SPI Bus. Below shows the descriptions on SPI bus.

4.1. Overview

The SPI interface provides high-speed data transfer capability with low power consumption for mobile electronic devices. The SPI bus was designed to operate on a point-to-multipoint basis by providing a separate, active-low chip select (CS) per device.

4.2. SPI Interface Description

In order to facilitate a broad implementation, the protocol is half duplex and does not require simultaneous operation of data OUT (DO) and data IN (DI). All TI communication devices are slaves in this protocol, and all transactions are initiated by the host, as the SPI Master. The clock rate for each one of the connected devices may be different and configured per device. Figure 3 shows SPI interface signals

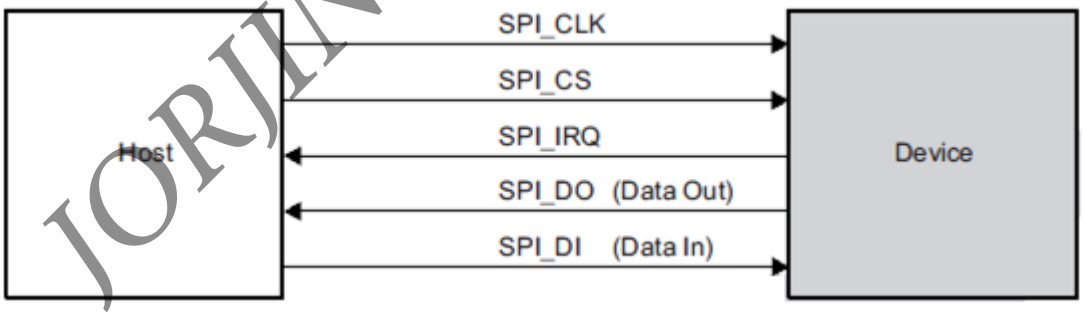


Figure 3 SPI Interface signals

4.3. SPI Line Description

Port Name	I/O	Description
SPI_CLK	I	Clock (0 MHz to 38.4 MHz) from host to slave
SPI_DI	I	Data from host to slave
SPI_CS(1)	I	CS signal from host to slave
SPI_IRQ(2)	O	Interrupt from slave to host
SPI_DO	O	Data from slave to host

(1) CS selects a CC3000 device, indicating that a master wants to communicate to the device.

(2) IRQ is a dual-purpose slave to the master direction line: in SPI IDLE state while no data transfer is active, driving IRQ low indicates to the master that the CC3000 device has data to pass to it; driving IRQ low following CS deassertion indicates that the CC3000 device is ready to receive data.

Table 5 SPI Interface Signals Description

4.4. SPI Timing

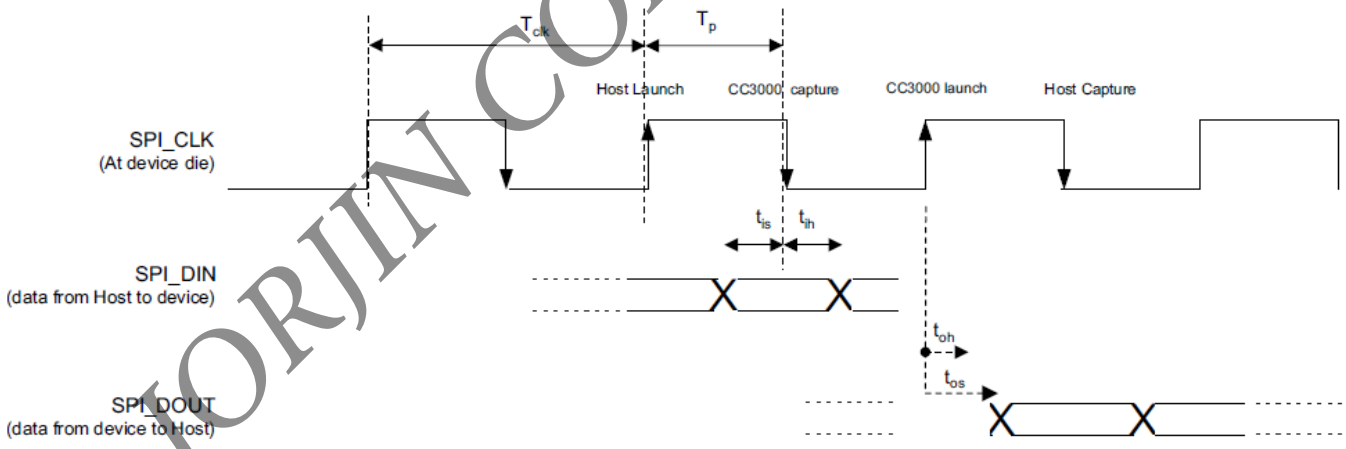


Figure 4 SPI Timing

Symbol	Parameter	Min	Max	Unit
T_{clk}	Clock period	62.5		ns
T_p	High pulse width (including jitter and duty cycle)	25(3)	37.5(3)	ns
t_{is}	RX setup time; minimum time in which data is stable before capture edge	5		ns
t_{ih}	RX hold time; minimum time in which data is stable after capture edge	5		
t_{os}	TX setup propagation time; maximum time from launch edge until data is stable		10.2	
t_{oh}	TX hold propagation time; minimum time of data stable after launch edge	3		
C_L	Capacitive load on I/F		20	pF

(1) The CS signal is considered to be asynchronous

(2) In the scheme above, the launching is on rise edge, and capturing is on fall edge. It can be configured to be the opposite

(3) 40% - 60% dc (valid for the minimum clock period)

Table 6 SPI Timing

5. POWER-UP SEQUENCE

Figure 7 demonstrates the wake up sequence of WG1300-B0

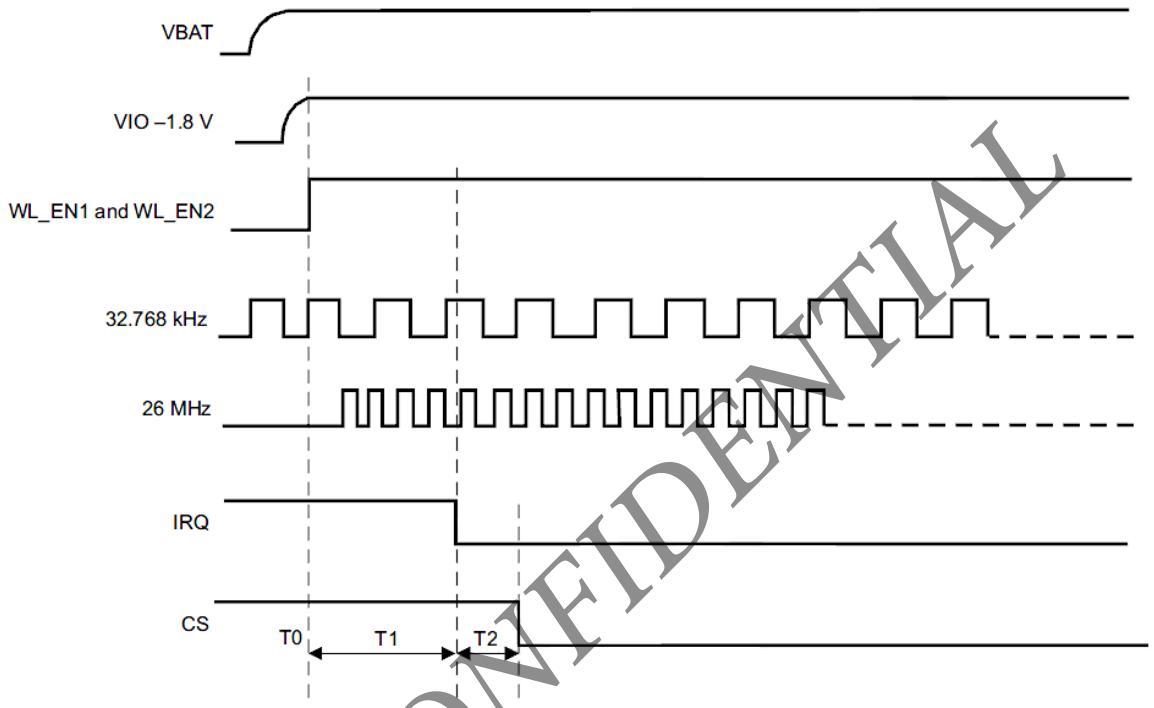


Figure 5 WG1300-B0 Power-On Sequences

Note:

1. VBAT_IN, VIO, and SLOWCLK must be available before WL_EN1 and WL_EN2 are asserted.
2. At T0: WL_EN1 and WL_EN2 can be asserted after the VIO reaches 90 percent of VIO voltage. On this functional mode the MCU drives the WLAN pins to initiate the power up (WL_EN1 and WL_EN2 are shorted and connected to MCU GPIO).
3. At T1 (wake-up time): The CC3000 device accomplishes power up after the IRQ changes state to LOW. Wake-up time T1 is approximately 53 msec.
4. At T2: The normal master SPI write sequence is CS low, followed by IRQ low (CC3000 host), indicating that the CC3000 core device is ready to accept data. The duration of T2 is approximately 7 msec.

6. DEBUG INTERFACE

The debug interface helps customers to evaluate the HW/SW features for their application. It also helps to debug during the development and manufacturing stage. The WG1300-B0 module support RS232 signals and UART signals for debug purpose. Connect RS232 and UART signals to the test points for future debug support.

6.1. UART Debug Lines

A unidirectional UART lines are provided for debugging WLAN subsystem and network subsystem functions. This is a TX-only debug interface that delivers diagnostic messages. Table 11 shows the dedicated UART debug pins of WG1300-B0

Signal names	WG1300-B0 Pin#	Function
WL_UART_DBG	4	Logger for WLAN FW debug
NS_UARTD	2	Networking subsystem UART Debug line

Table 7 WG1300-B0 UART Debug Lines

6.2. RS232 Debug Lines

During production testing the pins below are used for RTTT Wireless LAN SW utility. Table 12 shows the dedicated rs232 debug pins of WG1300-B0

Signal names	Function
WL_RS232_TX	RTTT Test Utility for WLAN RF Debug
WL_RS232_RX	

Table 8 WG1300-B0 RS232 Debug Lines

7. SMT AND BAKING RCOMMENDATIONS

7.1. Baking Condition

- Follow MSL Level 4 to do baking process.
- After bag is opened, devices that will be subjected to reflow solder or other high temperature process must be mounted within 72 hours of factory conditions <30°C/60% RH or stored at <10% RH.
- Device require bake, before mounting, if Humidity Indicator Card reads > 10%
- If baking is required, Devices may be baked for 8 hrs at 125°C.

7.2. SMT Recommendation

Figure 8 is recommended reflow profile and Table 13 is its information

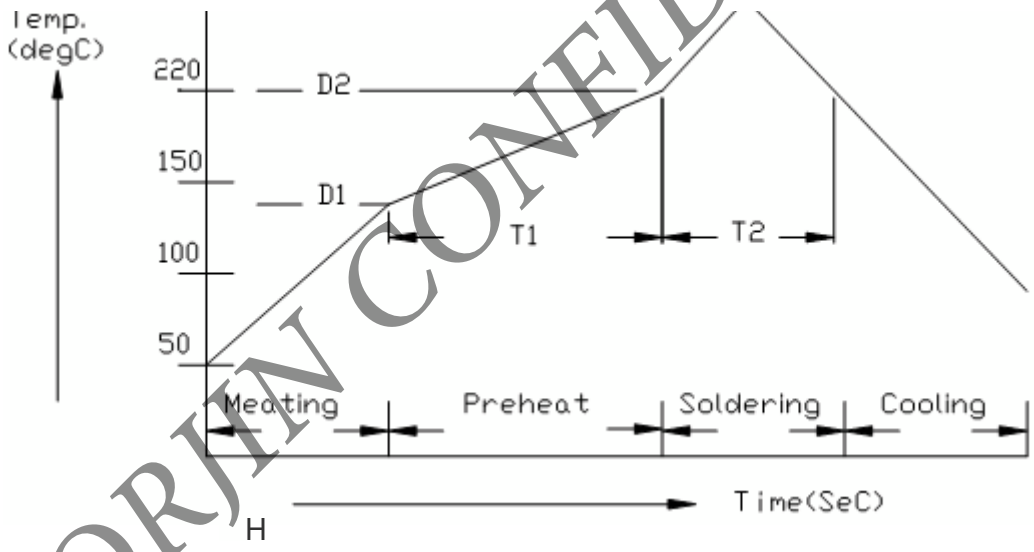


Figure 6 WG1300-B0 Recommended reflow profile

No.	Item	Temperature (°C)	Time (sec)
1	Pre-heat	D1: 140 ~ D2: 200	T1: 80 ~ 120
2	Soldering	D2: = 220	T2: 60 +/- 10
3	Peak-Temp.	D3: 250 °C max	

Table 9 WG1300-B0 reflow information

Note: (1) Reflow soldering is recommended two times maximum.
(2) Add Nitrogen while Reflow process: SMT solder ability will be better.

7.3. Stencil Thickness

0.1~ 0.15 mm (Recommended)

7.4. Soldering Paste (without Pb)

Recommended SENJU N705-GRN3360-K2-V can get better soldering effects.

8. PACKAGE INFORMATION

8.1. Module Mechanical Outline

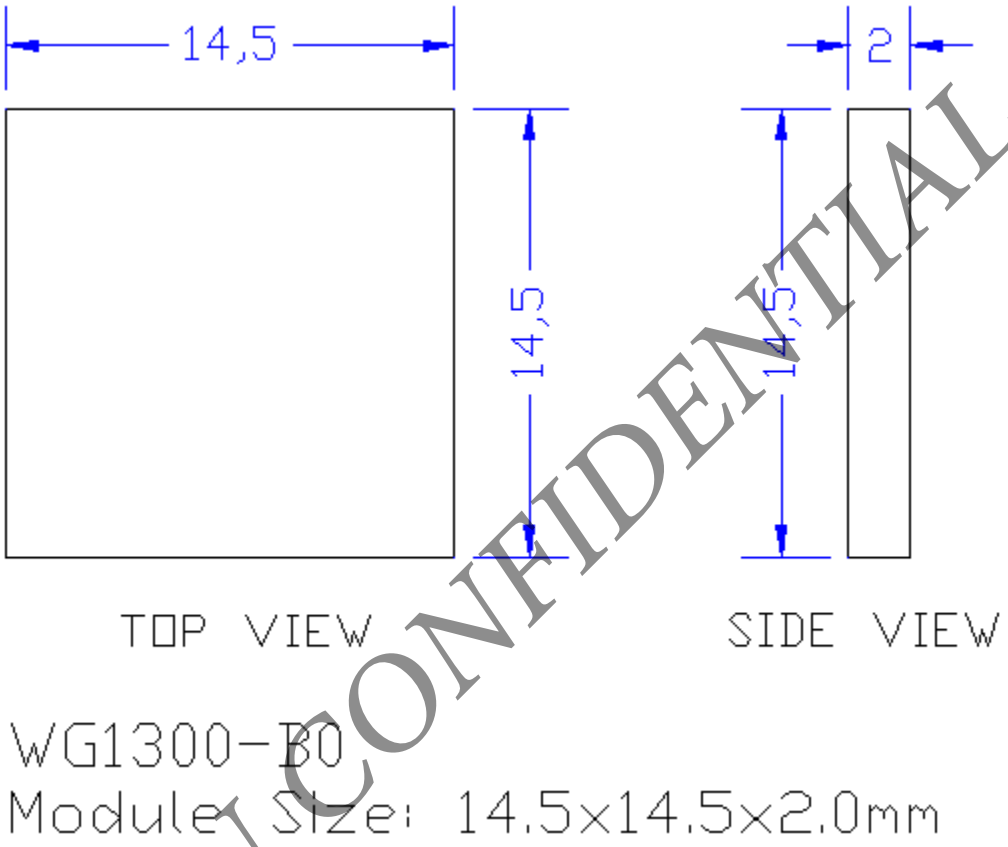
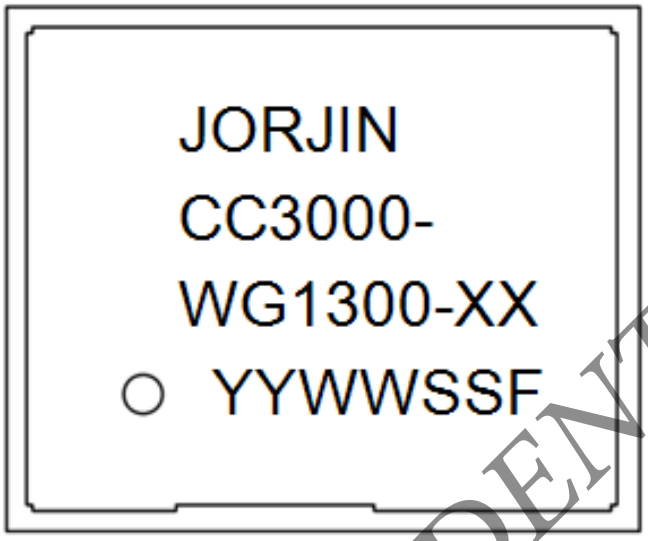


Figure 7 WG1300-B0 Mechanical Outline

8.2. Package Marking



Date Code: **YYWWSSF**

YY = Digit of the year, ex: 2010=10

WW = Week (01~53)

SS = Serial number from 01 ~99 match to manufacture's lot number

F = Reserve for internal use

Figure 8 WG1300-B0 Package Marking

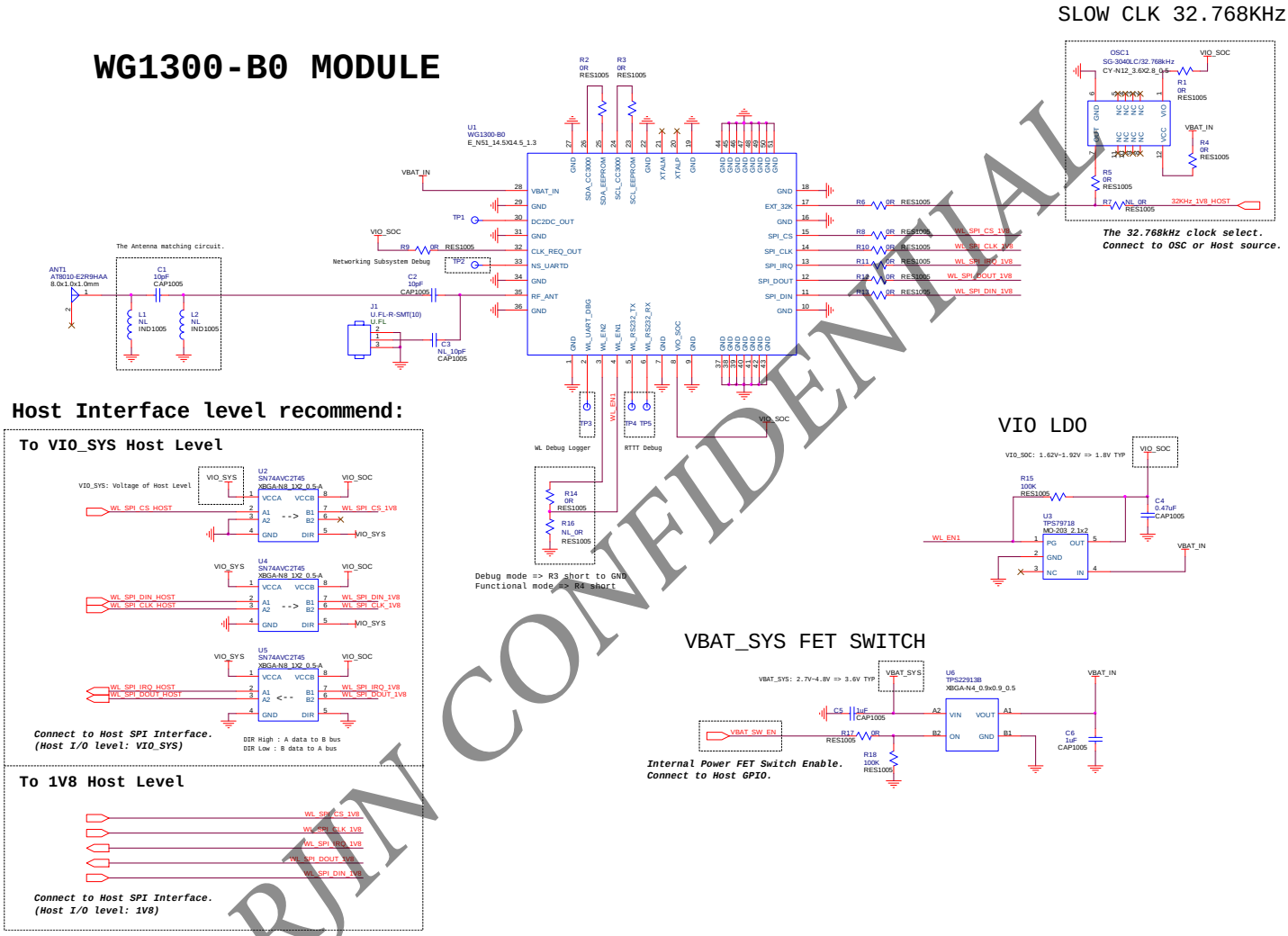
8.3. Ordering Informaiton

Order Number	Description
WG1300-B0	JORJIN CC3000 Module

Table 10 Orderable WG1300-B0 Part Numbers

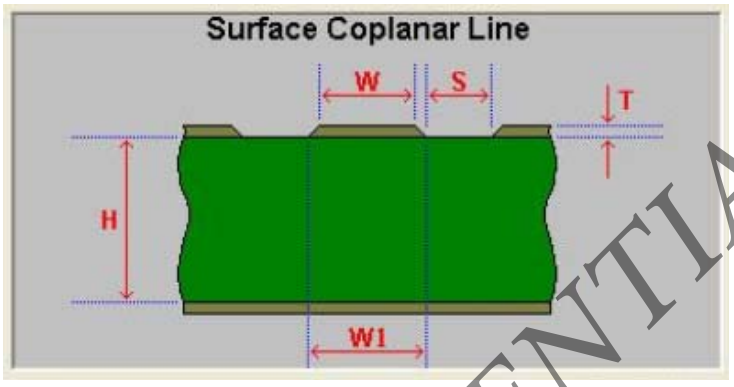
9. REFERENCE SCHEMATICS

WG1300-B0 to Host Reference Design



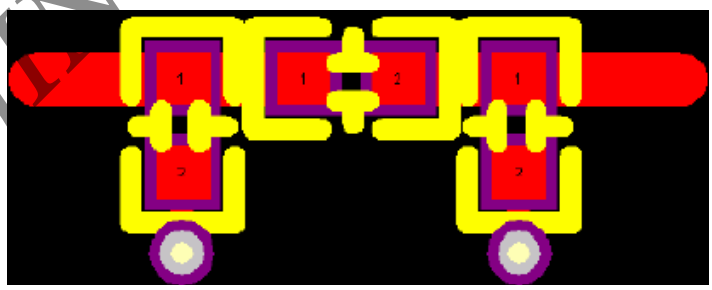
10. LAYOUT RECOMMENDATION

- **RF Trace & Antenna**
  - 50 ohm trace impedance match on the trace to the antenna.
  - Recommended 50ohm trace design for PCB layout



Height Between L1 and L2 **(H):**	12.0 mil
Trace **(W):**	14.3 mil
(W1):	14.3 mil
Thickness **(T):**	2.1 mil
Separation **(S):**	10.0 mil
Dielectric **(Er):**	4.3

  - Move all the high-speed traces and components far away from the antenna.
  - Check ANT vendor for the layout guideline and clearance.
  - Matching circuit layout should be as following figure.



- **Power Trace**
  - Power trace for VBAT_IN should be 40mil wide. 1.8V trace should be 18mil wide.
- **Ground**
  - Having a complete Ground and more GND vias under module in layer1 for

system stable and thermal dissipation as following figure.

- Have a complete Ground pour in layer 2 for thermal dissipation.
- Increase the GND pour in the 1st layer, move all the traces from the 1st layer to the inner layers if possible.
- Move GND vias close to the pad.

- **Slow Clock**
  - The slow clock trace should not be routed above or below digital signals on other layers.

- Add test points as the list below

Pin name
DC2DC_OUT
NS_UARTD
WL_UART_DBG
WL_RS232_TX
WL_RS232_RX

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11. HISTORY CHANGES

Revision	Date	Description
D 0.1	2012/9/8	Release 0.1
D 0.2	2012/10/12	1. Add module picture 2. Delete Sales contact information