



PCA8537

Automotive LCD driver for multiplex rates up to 1:8

Rev. 2 — 7 April 2015

Product data sheet

1. General description

The PCA8537 is a fully featured Liquid Crystal Display (LCD)¹ driver, specifically designed for high-contrast Vertical Alignment (VA) LCD with multiplex rates up to 1:8. It generates the drive signals for any static or multiplexed LCD containing up to eight backplanes, 46 segments, and up to 352 elements. The PCA8537 features an internal charge pump with internal capacitors for on-chip generation of the LCD driving voltage. To ensure an optimal and stable contrast over the full temperature range, the PCA8537 offers a programmable temperature compensation of the LCD supply voltage. The PCA8537 can be easily connected to a microcontroller by either the two-line I²C-bus (PCA8537AH) or a three-line bidirectional SPI-bus (PCA8537BH).

For a selection of NXP LCD segment drivers, see [Table 43 on page 72](#).

2. Features and benefits

- AEC Q100 compliant for automotive applications.
- Low-power single-chip LCD controller and driver
- 352 elements allowing to drive:
 - ◆ up to 44 7-segment alphanumeric characters
 - ◆ up to 22 14-segment alphanumeric characters
- Selectable backplane drive configuration: static, 2, 4, 6, or 8 backplane multiplexing
- Software programmable internal charge pump for on-chip LCD voltage generation up to 9 V with internal capacitors
- 400 kHz I²C-bus interface (PCA8537AH)
- 5 MHz SPI-bus interface (PCA8537BH)
- Programmable temperature compensation of V_{LCD} in four regions
- Selectable display bias configuration
- Wide range for digital power supply: from 1.8 V to 5.5 V
- Wide LCD supply range: from 2.5 V for low threshold LCDs and up to 9.0 V for high threshold twisted nematic LCDs
- Display memory bank switching in static, duplex, and quadruplex drive modes
- 352-bit RAM for display data storage
- Programmable frame frequency in the range of 60 Hz to 300 Hz in steps of 10 Hz; factory calibrated
- Integrated temperature sensor with temperature readout
- On chip calibration of internal oscillator frequency and V_{LCD}
- Manufactured in silicon gate CMOS process

1. The definition of the abbreviations and acronyms used in this data sheet can be found in [Section 20](#).



3. Applications

- Instrument cluster
- Car radio
- Climate control units

4. Ordering information

Table 1. Ordering information

| Type number | Interface type | Package | | |
|-------------|----------------------|---------|--|----------|
| | | Name | Description | Version |
| PCA8537AH | I ² C-bus | TQFP64 | plastic thin quad flat package; 64 leads; body 10 × 10 × 1.0 mm | SOT357-1 |
| PCA8537BH | SPI-bus | TQFP64 | plastic thin quad flat package; 64 leads; body 10 × 10 × 1.0 mm | SOT357-1 |

4.1 Ordering options

Table 2. Ordering options

| Product type number | Orderable part number | Sales item (12NC) | Delivery form | IC revision |
|---------------------|-----------------------|-------------------|----------------------------------|-------------|
| PCA8537AH/Q900/1 | PCA8537AH/Q900/1,5 | 935297895518 | tape and reel, 13 inch, dry pack | 1 |
| PCA8537BH/Q900/1 | PCA8537BH/Q900/1,5 | 935297896518 | tape and reel, 13 inch, dry pack | 1 |

5. Marking

Table 3. Marking codes

| Type number | Marking code |
|------------------|--------------|
| PCA8537AH/Q900/1 | PCA8537AH |
| PCA8537BH/Q900/1 | PCA8537BH |

6. Block diagram

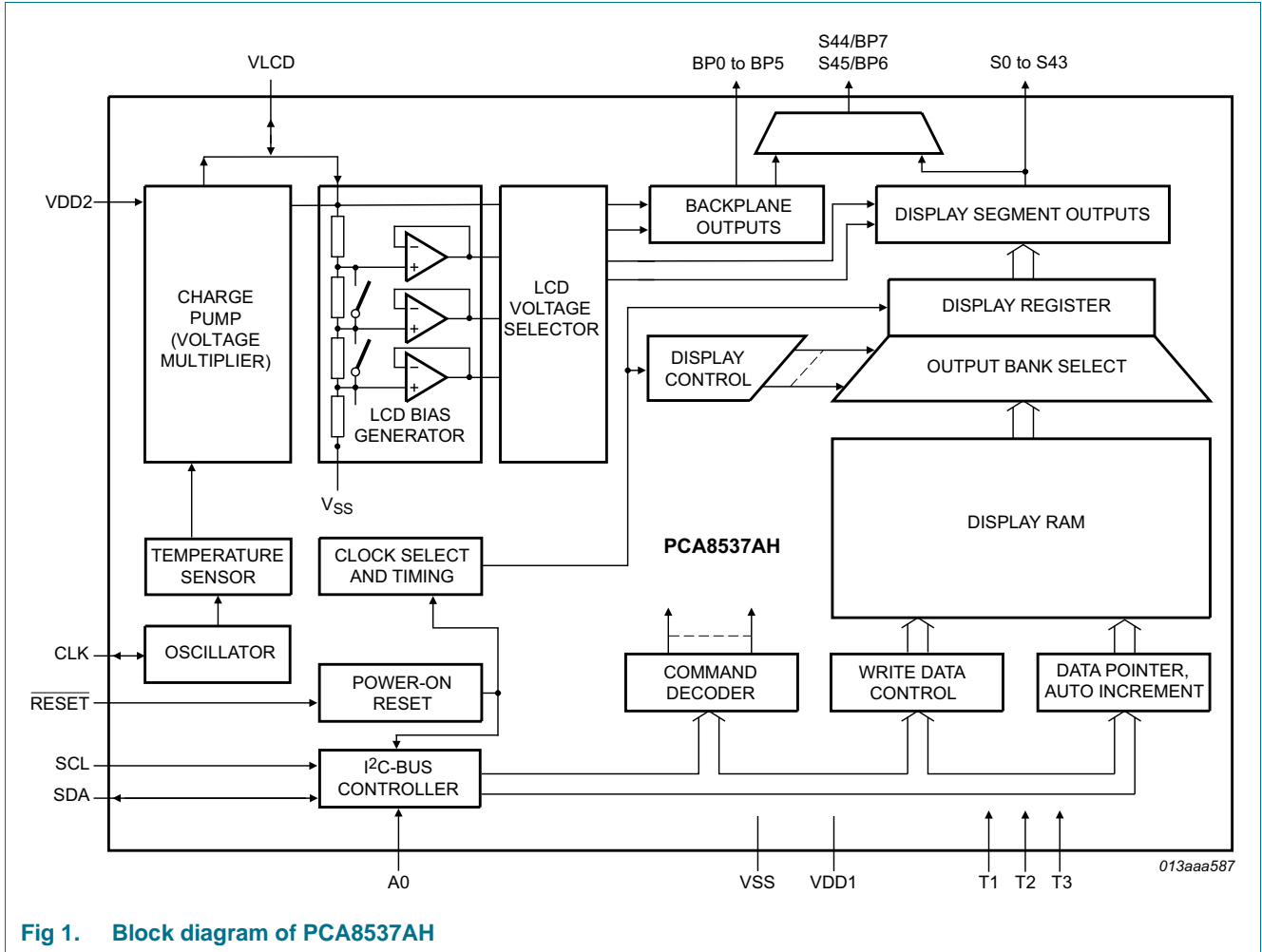


Fig 1. Block diagram of PCA8537AH

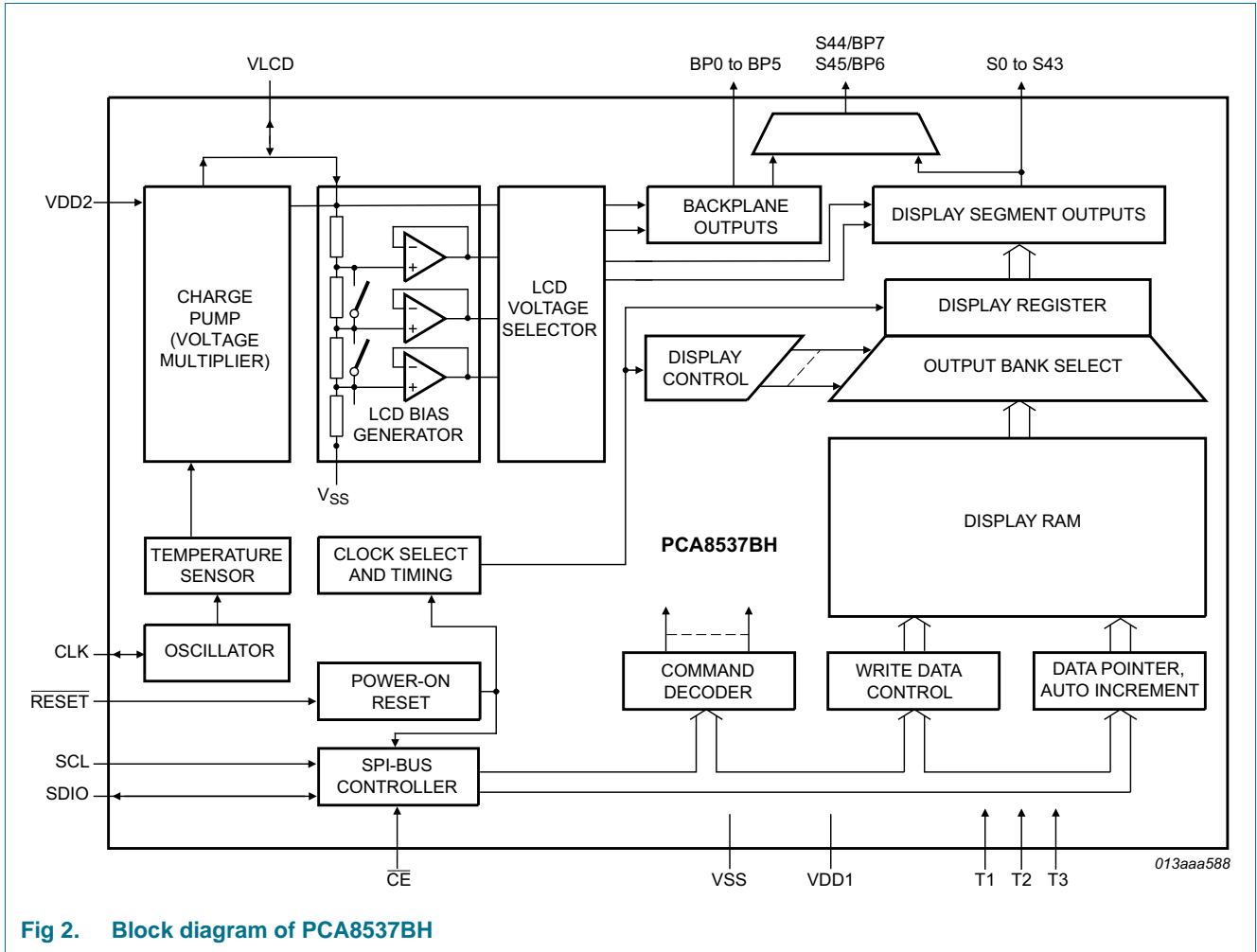


Fig 2. Block diagram of PCA8537BH

7.2 Pin description

Table 4. Pin description of PCA8537AH and PCA8537BH

Input or input/output pins must always be at a defined level (V_{SS} or V_{DD}) unless otherwise specified.

| Pin | Symbol | | Type | Description |
|---------------|---------------------------|------------------------|--------------|---|
| | PCA8537AH | PCA8537BH | | |
| 1 to 32 | S31 to S0 | | output | LCD segments |
| 33 | $\overline{\text{RESET}}$ | | input | active low reset input |
| 34 | SDA | | input/output | I ² C-bus serial data |
| | | $\overline{\text{CE}}$ | input | SPI-bus chip enable - active LOW |
| 35 | SCL | | input | I ² C-bus serial clock |
| | | SCL | input | SPI-bus serial clock |
| 36 | A0 | | input | I ² C-bus slave address selection |
| | | SDIO | input/output | SPI-bus serial data |
| 37, 38, 40 | T1 to T3 | | input | test pins; must be tied to V_{SS} in applications |
| 39 | CLK | | input/output | internal oscillator output, external oscillator input |
| 41 | VSS | | supply | ground supply |
| 42 | VDD1 | | supply | supply voltage 1 |
| 43 | VDD2 | | supply | supply voltage 2 |
| 44 | VLCD ^[1] | | supply | LCD supply ^[2] |
| 45 to 50 | BP0 to BP5 | | output | LCD backplanes |
| 51 | S45/BP6 | | output | LCD segments for 1:6 multiplex drive mode; |
| 52 | S44/BP7 | | output | LCD backplanes for 1:8 multiplex drive mode |
| 53 to 64 | S43 to S32 | | output | LCD segments |

[1] V_{LCD} must be equal to or greater than V_{DD2} .

[2] When the internal V_{LCD} generation is used, this pin drives the V_{LCD} voltage. In this case pin VLCD is an output. When the external supply is requested, then pin VLCD is an input and V_{LCD} can be supplied on it. In this case, the internal charge pump must be disabled (see [Table 9](#)).

8. Functional description

The PCA8537 is a versatile peripheral device designed to interface any microcontroller to a wide variety of LCDs. It can directly drive any static or multiplexed LCD containing up to 352 elements.

8.1 Commands of PCA8537

The commands to control the PCA8537 are defined in [Table 5](#). Any other combinations of operation code bits that are not mentioned in this document can lead to undesired operation modes of PCA8537.

Table 5. Commands of PCA8537

The bit labeled with - is not implemented.

| Command name | RS ^[1] | Bits | | | | | | | | Reference |
|-------------------|-------------------|---------|---|--------|--------|----------|----------|--------|-------------------------------|--------------------------------|
| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| Initialize | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | Section 8.1.1 |
| OTP-refresh | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | Section 8.1.2 |
| Oscillator-ctrl | 0 | 1 | 1 | 0 | 0 | 1 | 1 | COE | OSC | Section 8.1.3 |
| Charge-pump-ctrl | 0 | 1 | 1 | 0 | 0 | 0 | 0 | CPE | CPC | Section 8.1.4 |
| Temp-msr-ctrl | 0 | 1 | 1 | 0 | 0 | 1 | 0 | TCE | TME | Section 8.1.5 |
| Temp-comp | 0 | 0 | 0 | 0 | 1 | 1 | SLA[2:0] | | Section 8.1.6 | |
| | 0 | 0 | 0 | 1 | 0 | 0 | SLB[2:0] | | | |
| | 0 | 0 | 0 | 1 | 0 | 1 | SLC[2:0] | | | |
| | 0 | 0 | 0 | 1 | 1 | 0 | SLD[2:0] | | | |
| Set-VPR | 0 | 0 | 1 | 0 | 0 | VPR[7:4] | | | Section 8.1.7 | |
| | 0 | 0 | 1 | 0 | 1 | VPR[3:0] | | | | |
| Display-enable | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | E | Section 8.1.8 |
| Set-MUX-mode | 0 | 0 | 0 | 0 | 0 | 0 | M[2:0] | | Section 8.1.9 | |
| Set-bias-mode | 0 | 1 | 1 | 0 | 0 | 0 | 1 | B[1:0] | | Section 8.1.10 |
| Load-data-pointer | 0 | 1 | 0 | P[5:0] | | | | | | Section 8.1.11 |
| Frame-frequency | 0 | 0 | 1 | 1 | F[4:0] | | | | | Section 8.1.12 |
| Bank-select | 0 | 0 | 0 | 0 | 0 | 1 | 0 | IBS | OBS | Section 8.1.13 |
| Write-RAM-data | 1 | B[7:0] | | | | | | | | Section 8.1.14 |
| Temp-read | - | TD[7:0] | | | | | | | | Section 8.1.15 |
| Invmode_ctrl | 0 | 1 | 1 | 0 | 1 | 0 | 1 | LF | 0 | Section 8.1.16 |
| Temp-filter | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | TFE | Section 8.1.17 |

[1] For further information about the register selection bit, see [Table 31 on page 50](#).

8.1.1 Command: Initialize

This command generates a chip-wide reset which resets all command values to their default values. After this command is sent, it is possible to send additional commands without the need to re-initialize the interface. The reset takes 100 ns to complete.

Table 6. Initialize - initialize command bit description

For further information, see [Section 8.2 on page 16](#).

| Bit | Symbol | Binary value | Description |
|--------|--------|--------------|-------------|
| 7 to 0 | - | 00111010 | fixed value |

8.1.2 Command: OTP-refresh

During production and testing of the device, each IC is calibrated to achieve the specified accuracy of V_{LCD} , the frame frequency, and the temperature measurement. This calibration is performed on EPROM cells called One Time Programmable (OTP) cells.

The device reads these cells every time at power-on, after a reset, and every time when the initialize command or the OTP-refresh command is sent.

Remark: It is recommended not to enter power-down mode during the OTP refresh cycle.

Table 7. OTP-refresh - OTP-refresh command bit description

| Bit | Symbol | Binary value | Description |
|--------|--------|--------------|-------------|
| 7 to 0 | - | 11010000 | fixed value |

8.1.3 Command: Oscillator-ctrl

The Oscillator-ctrl command switches between internal and external oscillator and enables or disables the pin CLK.

Table 8. Oscillator-ctrl - oscillator control command bit description

For further information, see [Section 8.1.3.1](#).

| Bit | Symbol | Binary value | Description |
|--------|--------|------------------|---|
| 7 to 2 | - | 110011 | fixed value |
| 1 | COE | | control pin CLK |
| | | 0 ^[1] | clock signal not available on pin CLK; pin CLK is in 3-state and may be left floating |
| | | 1 | clock signal available on pin CLK |
| 0 | OSC | | oscillator source |
| | | 0 ^[1] | internal oscillator used |
| | | 1 | external oscillator used; pin CLK becomes an input |

[1] Default value.

8.1.3.1 Oscillator

The internal logic and LCD drive signals of the PCA8537 are timed either by the built-in oscillator or from an external clock.

8.1.3.2 Internal oscillator

When the internal oscillator is used, it is possible to make the clock signal available on pin CLK by using the Oscillator-ctrl command (see [Table 8](#)). If this is not intended, the pin CLK should be left open. At power-on the signal at pin CLK is disabled and pin CLK is in 3-state.

If the internal charge pump is enabled, then the internal oscillator starts and is used to run the charge pump. An external oscillator can still be applied for driving the display waveforms.

The duty cycle of the output clock provided on the CLK pin is not always 50 : 50. [Table 18 on page 13](#) shows the expected duty cycle for each of the chosen frame frequencies.

8.1.3.3 External clock

In applications where an external clock must be applied to the PCA8537, bit OSC (see [Table 8](#)) must be set logic 1. In this case, pin CLK becomes an input.

The CLK signal is a signal that is fed into the V_{DD1} domain. Therefore it must have an amplitude equal to the V_{DD1} voltage supplied to the chip and be referenced to V_{SS}.

The clock frequency (f_{clk}) determines the LCD frame frequency.

Remark: If an external clock is used then this clock signal must always be supplied to the device. Removing the clock can freeze the LCD in a DC state. Removal of the clock is possible when following the correct procedures (see [Figure 11 on page 21](#) and [Figure 12 on page 22](#)).

8.1.4 Command: Charge-pump-ctrl

The Charge-pump-ctrl command enables or disables the internal V_{LCD} generation and controls the charge pump voltage multiplier setting.

Table 9. Charge-pump-ctrl - charge pump control command bit description
For further information, see [Table 12 on page 11](#) and [Section 8.4.3 on page 26](#).

| Bit | Symbol | Binary value | Description |
|--------|--------|------------------|--|
| 7 to 2 | - | 110000 | fixed value |
| 1 | CPE | | charge pump switch |
| | | 0 ^[1] | charge pump disabled; no internal V _{LCD} generation; external supply of V _{LCD} |
| | | 1 | charge pump enabled |
| 0 | CPC | | charge pump voltage multiplier setting |
| | | 0 ^[1] | V _{LCD} = 2 × V _{DD2} |
| | | 1 | V _{LCD} = 3 × V _{DD2} |

[1] Default value.

8.1.5 Command: Temp-msr-ctrl

The Temp-msr-ctrl command enables or disables the temperature measurement block and the temperature compensation of V_{LCD} .

Table 10. Temp-msr-ctrl - temperature measurement control command bit description

For further information, see [Section 8.4.4 on page 28](#).

| Bit | Symbol | Binary value | Description |
|--------|--------|------------------|--|
| 7 to 2 | - | 110010 | fixed value |
| 1 | TCE | | temperature compensation switch |
| | | 0 | no temperature compensation of V_{LCD} possible |
| | | 1 ^[1] | temperature compensation of V_{LCD} possible |
| 0 | TME | | temperature measurement switch |
| | | 0 | temperature measurement disabled: no temperature readout possible |
| | | 1 ^[1] | temperature measurement enabled: temperature readout possible |

[1] Default value.

8.1.6 Command: Temp-comp

The Temp-comp command allows setting the temperature compensation coefficients for each of the temperature regions SFA to SFD. For further information, see [Section 8.4.4.2](#).

Table 11. Temp-comp - temperature compensation coefficients command

For further information, see [Section 8.4.4 on page 28](#).

| Bit | Symbol | Binary value | Description |
|------------|----------|---------------------------|---|
| SLA | | | |
| 7 to 3 | - | 00011 | fixed value |
| 2 to 0 | SLA[2:0] | 000 ^[1] to 111 | temperature compensation coefficient SLA , see Table 27 on page 30 |
| SLB | | | |
| 7 to 3 | - | 00100 | fixed value |
| 2 to 0 | SLB[2:0] | 000 ^[1] to 111 | temperature compensation coefficient SLB , see Table 27 on page 30 |
| SLC | | | |
| 7 to 3 | - | 00101 | fixed value |
| 2 to 0 | SLC[2:0] | 000 ^[1] to 111 | temperature compensation coefficient SLC , see Table 27 on page 30 |
| SLD | | | |
| 7 to 3 | - | 00110 | fixed value |
| 2 to 0 | SLD[2:0] | 000 ^[1] to 111 | temperature compensation coefficient SLD , see Table 27 on page 30 |

[1] Default value.

8.1.7 Command: Set-VPR

With these two instructions, it is possible to set the target V_{LCD} voltage for the internal charge pump.

Table 12. Set-VPR - set VPR command bit description

For further information, see [Section 8.4.2 on page 24](#).

| Bit | Symbol | Binary value | Description |
|--------------------|----------|--|--|
| Set-VPR MSB | | | |
| 7 to 4 | - | 0100 | fixed value |
| 3 to 0 | VPR[7:4] | 0000 ^[1] to 1111 ^[2] | the four most significant bits of VPR[7:0] |
| Set-VPR LSB | | | |
| 7 to 4 | - | 0101 | fixed value |
| 3 to 0 | VPR[3:0] | 0000 ^[1] to 1111 ^[2] | the four least significant bits of VPR[7:0] |

[1] Default value.

[2] VPR[7:0] = 0h results in $V_{prog(LCD)} = 3\text{ V}$;
VPR[7:0] = C8h results in $V_{prog(LCD)} = 9\text{ V}$.

8.1.8 Command: Display-enable

This command allows switching the display on and off. The possibility to disable and enable the display allows implementation of blinking the entire display under external control.

Table 13. Display-enable - display enable command bit description

| Bit | Symbol | Binary value | Description |
|--------|--------|------------------|---|
| 7 to 1 | - | 0011100 | fixed value |
| 0 | E | 0 ^[1] | display disabled backplane and segment outputs are internally connected to V_{SS} |
| | | 1 | display enabled |

[1] Default value.

8.1.9 Command: Set-MUX-mode

The multiplex drive mode is configured with the bits described in [Table 14](#).

Table 14. Set-MUX-mode - set multiplex drive mode command bit description

For further information, see [Section 8.4.5 on page 31](#).

| Bit | Symbol | Binary value | Description |
|--------|--------|--------------------|---|
| 7 to 3 | - | 00000 | fixed value |
| 2 to 0 | M[2:0] | 000 ^[1] | 1:8 multiplex drive mode 8 backplanes and 44 segments |
| | | 011 | |
| | | 101 | |
| | | 111 | |
| | | 110 | 1:6 multiplex drive mode 6 backplanes and 46 segments |
| | | 100 | 1:4 multiplex drive mode 4 backplanes and 44 segments |
| | | 010 | 1:2 multiplex drive mode 2 backplanes and 44 segments |
| | | 001 | static drive mode 1 backplane and 44 segments |

[1] Default value.

8.1.10 Command: Set-bias-mode

The Set-bias-mode command allows setting the bias level.

Table 15. Set-bias-mode - set bias mode command bit description

For further information, see [Section 8.4.5 on page 31](#).

| Bit | Symbol | Binary value | Description |
|--------|--------|-------------------|---------------------------------------|
| 7 to 2 | - | 110001 | fixed value |
| 1 to 0 | B[1:0] | | LCD bias configuration ^[1] |
| | | 00 ^[2] | $\frac{1}{4}$ bias |
| | | 01 | |
| | | 11 | $\frac{1}{3}$ bias |
| | | 10 | $\frac{1}{2}$ bias |

[1] Not applicable for static drive mode.

[2] Default value.

8.1.11 Command: Load-data-pointer

The Load-data-pointer command defines the display RAM address where the following display data will be sent to.

Table 16. Load-data-pointer - load data pointer command bit description

For further information, see [Section 8.8 on page 43](#).

| Bit | Symbol | Binary value | Description |
|--------|--------|---------------------|---|
| 7 to 6 | - | 10 | fixed value |
| 5 to 0 | P[5:0] | 000000 to 101101 | RAM address 6-bit binary value of 0 to 45 |

8.1.12 Command: Frame-frequency

With the Frame-frequency command, the frame frequency and the output clock frequency can be configured.

Table 17. Frame frequency - frame frequency and output clock frequency command bit description

| Bit | Symbol | Binary value | Description |
|--------|--------|------------------------------|--|
| 7 to 5 | - | 011 | fixed value |
| 4 to 0 | F[4:0] | see Table 18 | frame frequency values, see Table 18 |

Table 18. Frame frequency values

| F[4:0] | Nominal frame frequency f_{fr} (Hz) ^[1] | Resultant output clock frequency, $f_{clk(o)}$ (Hz) | Duty cycle (%) ^[2] |
|----------------------|--|---|-------------------------------|
| 00000 | 60 | 2880 | 20 : 80 |
| 00001 | 70 | 3360 | 7 : 93 |
| 00010 | 80 | 3840 | 47 : 53 |
| 00011 | 91 | 4368 | 40 : 60 |
| 00100 | 100 | 4800 | 33 : 67 |
| 00101 | 109 | 5232 | 27 : 73 |
| 00110 | 120 | 5760 | 20 : 80 |
| 00111 | 129.7 | 6226 | 13 : 87 |
| 01000 | 141.2 | 6778 | 5 : 95 |
| 01001 | 150 | 7200 | 50 : 50 |
| 01010 | 160 | 7680 | 47 : 53 |
| 01011 | 171.4 | 8227 | 43 : 57 |
| 01100 | 177.8 | 8534 | 41 : 59 |
| 01101 | 192 | 9216 | 36 : 64 |
| 01110 ^[3] | 200 | 9600 | 33 : 67 |
| 01111 | 208.7 | 10018 | 30 : 70 |
| 10000 | 218.2 | 10474 | 27 : 73 |
| 10001 | 228.6 | 10973 | 23 : 77 |
| 10010 | 240 | 11520 | 20 : 80 |
| 10011 | 252.6 | 12125 | 16 : 84 |
| 10100, 10101 | 266.7 | 12802 | 10 : 90 |
| 10110, 10111 | 282.4 | 13555 | 5 : 95 |
| 11000 to 11111 | 300 | 14400 | 50 : 50 |

[1] Nominal frame frequency calculated for the default clock frequency of 9600 Hz.

[2] Duty cycle definition: % HIGH-level time : % LOW-level time.

[3] Default value.

8.1.12.1 Timing and frame frequency

The timing of the PCA8537 organizes the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs. The timing also generates the LCD frame frequency. The frame frequency is a fixed division of the internal clock or of the frequency applied to pin CLK when an external clock is used.

When the internal clock is used, the clock frequency can be programmed by software such that the nominal frame frequency can be chosen in steps of 10 Hz in the range of 60 Hz to 300 Hz (see [Table 18](#)). Furthermore the nominal frame frequency is factory-calibrated with an accuracy of ±15 %.

When the internal clock is enabled at pin CLK by using bit COE, the duty ratio of the clock may change when choosing different values for the frame frequency prescaler. [Table 18](#) shows the different output duty ratios for each frame frequency prescaler setting.

8.1.13 Command: Bank-select

For the multiplex drive modes 1:4, 1:2, and the static drive mode, it is possible to write data to one area of the RAM while displaying from another. These areas are named RAM banks. There are two banks, 0 and 1. [Figure 39 on page 49](#) and [Figure 40 on page 49](#) show the concept. The Bank-select command controls where data is written to and where it is displayed from.

Table 19. Bank-select - bank select command bit description

For further information, see [Section 8.9 on page 49](#).

| Bit | Symbol | Binary value | Description |
|--------|--------|------------------|---|
| 7 to 2 | - | 000010 | fixed value |
| 1 | IBS | | selects RAM bank to write to |
| | | 0 ^[1] | Bank 0 |
| | | 1 | Bank 1 |
| 0 | OBS | | selects RAM bank to read from to the LCD |
| | | 0 ^[1] | Bank 0 |
| | | 1 | Bank 1 |

[1] Default value.

8.1.14 Command: Write-RAM-data

By setting the RS bit of the control byte to logic 1, all data transferred is interpreted as RAM data and placed in the RAM in accordance with the current setting of the RAM address pointer (see [Section 8.1.11 on page 12](#)). Definition of the RS can be found in [Table 31 on page 50](#).

Remark: After Power-On Reset (POR) the RAM content is random and should be brought to a defined status by clearing it (setting it to logic 0).

Table 20. Write-RAM-data - write RAM data command bit description

For further information, see [Section 8.8 on page 43](#).

| Bit | Symbol | Binary value | Description |
|--------|--------|----------------------|--|
| 7 to 0 | B[7:0] | 00000000 to 11111111 | writing data byte-wise to the RAM |

8.1.15 Command: Temp-read

The Temp-read command allows reading out the temperature values measured by the internal temperature sensor.

Table 21. Temp-read - temperature readout command bit description

For further information, see [Section 8.4.4 on page 28](#).

| Bit | Symbol | Binary value | Description |
|--------|---------|----------------------|---|
| 7 to 0 | TD[7:0] | 00000000 to 11111111 | digital temperature values ^[1] |

[1] For this command, bit $\overline{R/W}$ of the I²C-bus slave address byte has to be set logic 1 (see [Table 32](#)).

8.1.16 Command: Invmode_ctrl

The Invmode_ctrl command allows changing the drive scheme inversion mode.

The waveforms used to drive LCD displays inherently produce a DC voltage across the display cell. The PCA8537 compensates for the DC voltage by inverting the waveforms on alternate frames or alternate lines. The choice of compensation method is determined with the LF bit.

Table 22. Invmode_ctrl - drive scheme inversion command bit description

For further information, see [Section 8.4.6 on page 34](#).

| Bit | Symbol | Binary value | Description |
|--------|--------|------------------|--|
| 7 to 2 | - | 110101 | fixed value |
| 1 | LF | | set inversion mode |
| | | 0 ^[1] | driving scheme A: line inversion mode |
| | | 1 | driving scheme B: frame inversion mode |
| 0 | - | 0 | fixed value |

[1] Default value.

In frame inversion mode, the DC value is compensated across two frames and not within one frame. Changing the inversion mode to frame inversion reduces the power consumption, therefore it is useful when power consumption is a key point in the application.

Frame inversion may not be suitable for all applications. The RMS voltage across a segment is better defined, however since the switching frequency is reduced there is possibility for flicker to occur.

[Figure 24 on page 34](#) to [Figure 30 on page 40](#) are showing the waveforms in line inversion mode. [Figure 31 on page 41](#) shows an example of frame inversion.

8.1.17 Command: Temp-filter

Table 23. Temp-filter - digital temperature filter command bit description

For further information, see [Section 8.4.4 on page 28](#).

| Bit | Symbol | Binary value | Description |
|--------|--------|------------------|--|
| 7 to 1 | - | 1101001 | fixed value |
| 0 | TFE | | digital temperature filter switch |
| | | 0 ^[1] | digital temperature filter disabled; the unfiltered digital value of TD[7:0] is immediately available for the readout and V _{LCD} compensation, see Section 8.4.4.1 |
| | | 1 | digital temperature filter enabled |

[1] Default value.

8.2 Start-up and shut-down

8.2.1 Power-On Reset (POR)

At power-on, the PCA8537 resets to starting conditions as follows:

1. All backplane and segment outputs are set to V_{SS}.
2. Selected drive mode is: 1:8 with 1/4 bias.
3. Input and output bank selectors are reset.
4. The I²C-bus and SPI-bus interface are initialized.
5. The data pointer is cleared (set logic 0).
6. The internal oscillator is running; no clock signal is available on pin CLK; pin CLK is in 3-state.
7. Temperature measurement is enabled.
8. Temperature filter is disabled.
9. The internal V_{LCD} voltage generation is disabled. The charge pump is switched off.
10. The V_{LCD} temperature compensation is enabled.
11. The display is disabled.

The reset state is as shown in [Table 24](#).

Table 24. Reset state

Reset state of configuration bits shown in the command table format for clarity. The bit labeled with - has an undefined reset state.

| Command name | Bits | | | | | | | |
|-------------------|------|---|---------------------|----------------|-----------------|----------------|-------------|---------|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Oscillator-ctrl | 1 | 1 | 0 | 0 | 1 | 1 | COE = 0 | OSC = 0 |
| Charge-pump-ctrl | 1 | 1 | 0 | 0 | 0 | 0 | CPE = 0 | CPC = 0 |
| Temp-msr-ctrl | 1 | 1 | 0 | 0 | 1 | 0 | TCE = 1 | TME = 1 |
| Temp-comp | 0 | 0 | 0 | 1 | 1 | SLA[2:0] = 000 | | |
| | 0 | 0 | 1 | 0 | 0 | SLB[2:0] = 000 | | |
| | 0 | 0 | 1 | 0 | 1 | SLC[2:0] = 000 | | |
| | 0 | 0 | 1 | 1 | 0 | SLD[2:0] = 000 | | |
| Set-VPR | 0 | 1 | 0 | 0 | VPR[7:4] = 0000 | | | |
| | 0 | 1 | 0 | 1 | VPR[3:0] = 0000 | | | |
| Display-enable | 0 | 0 | 1 | 1 | 1 | 0 | 0 | E = 0 |
| Set-MUX-mode | 0 | 0 | 0 | 0 | 0 | M[2:0] = 000 | | |
| Set-bias-mode | 1 | 1 | 0 | 0 | 0 | 1 | B[1:0] = 00 | |
| Load-data-pointer | 1 | 0 | P[5:0] is undefined | | | | | |
| Frame-frequency | 0 | 1 | 1 | F[4:0] = 01110 | | | | |
| Bank-select | 0 | 0 | 0 | 0 | 1 | 0 | IBS = 0 | OBS = 0 |
| Invmode_ctrl | 1 | 1 | 0 | 1 | 0 | 1 | LF = 0 | - |
| Temp-filter | 1 | 1 | 0 | 1 | 0 | 0 | 1 | TFE = 0 |

Remark: Do not transfer data on the I²C-bus or SPI-bus for at least 1 ms after a power-on reset to allow the reset action to complete.

The first command sent to the device after the power-on event must be the Initialize command (see [Section 8.1.1](#)).

After POR and before enabling the display, the RAM content should be brought to a defined status

- by clearing it (setting it all to logic 0) or
- by writing meaningful content (for example, a graphic)

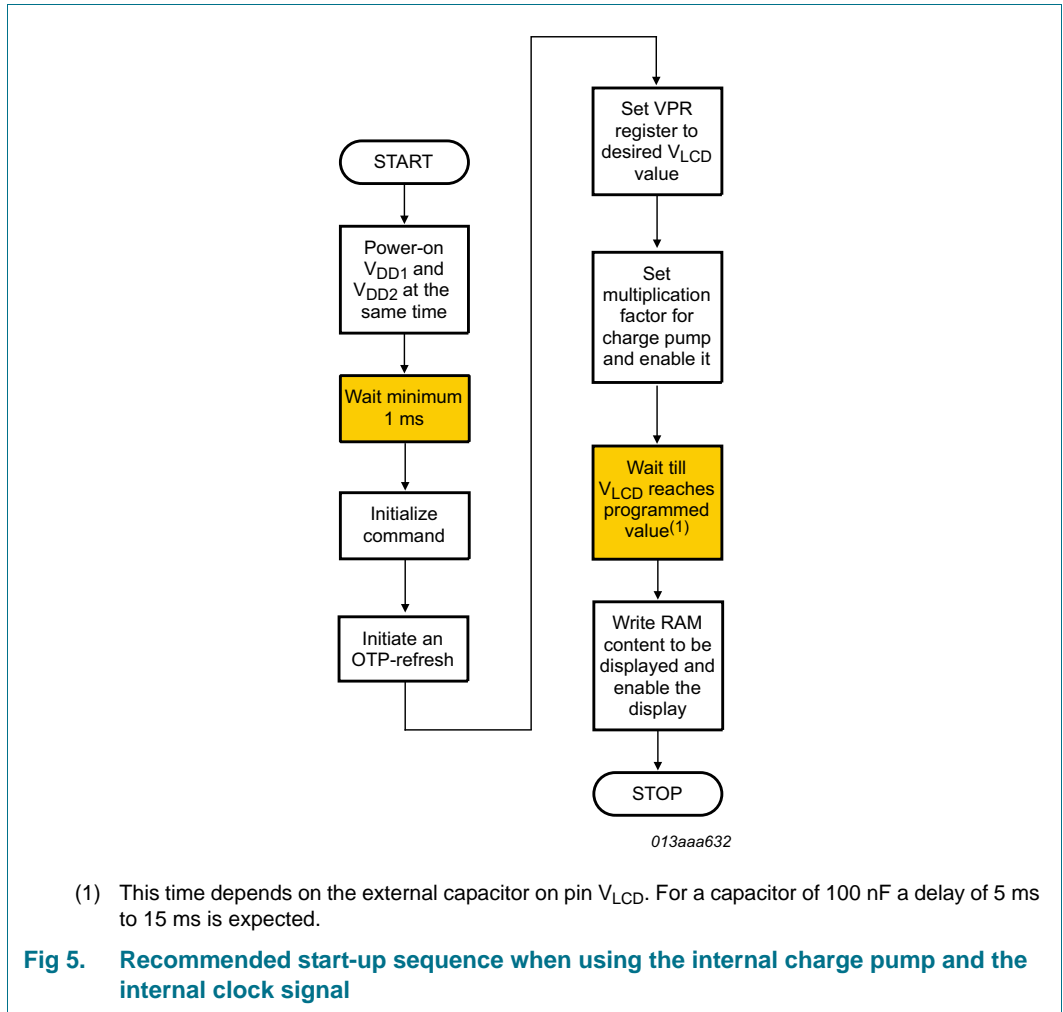
otherwise unwanted display artifacts may appear on the display.

8.2.2 RESET pin function

The $\overline{\text{RESET}}$ pin of the PCA8537 resets all the registers to their default state. The reset state is given in [Table 24](#). The RAM contents remain unchanged. After the reset signal is removed, the PCA8537 will behave in the same manner as after POR. See [Section 8.2.1](#) for details.

8.2.3 Recommended start-up sequences

This chapter describes how to proceed with the initialization of the chip in different application modes.



If the display is enabled too soon after the charge pump is enabled, then the V_{LCD} voltage may not have yet stabilized leading to an uneven display effect.

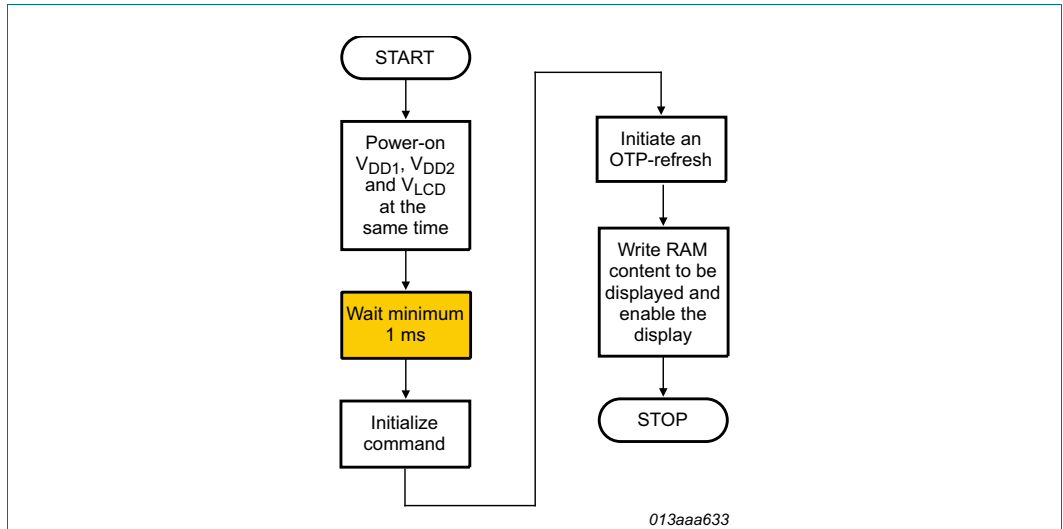
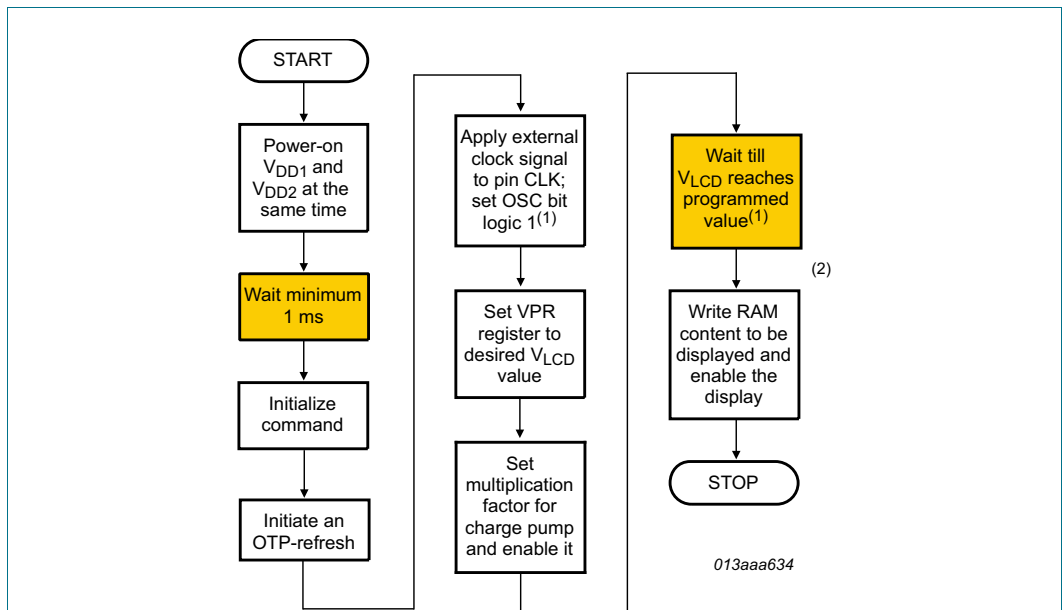
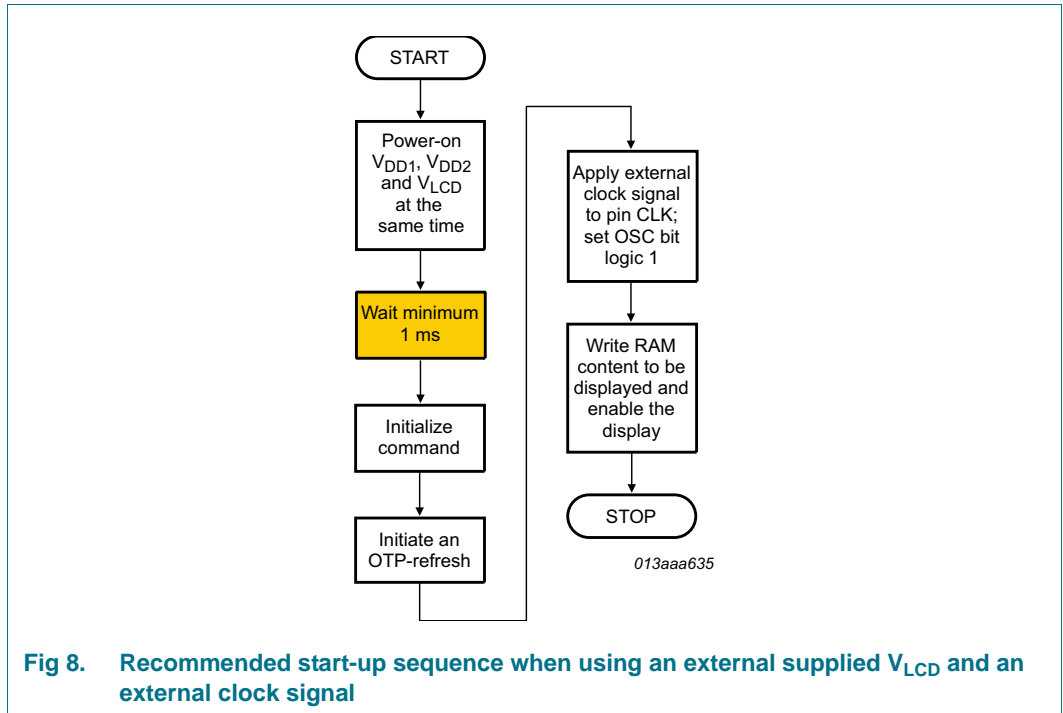


Fig 6. Recommended start-up sequence when using an external supplied V_{LCD} and the internal clock signal



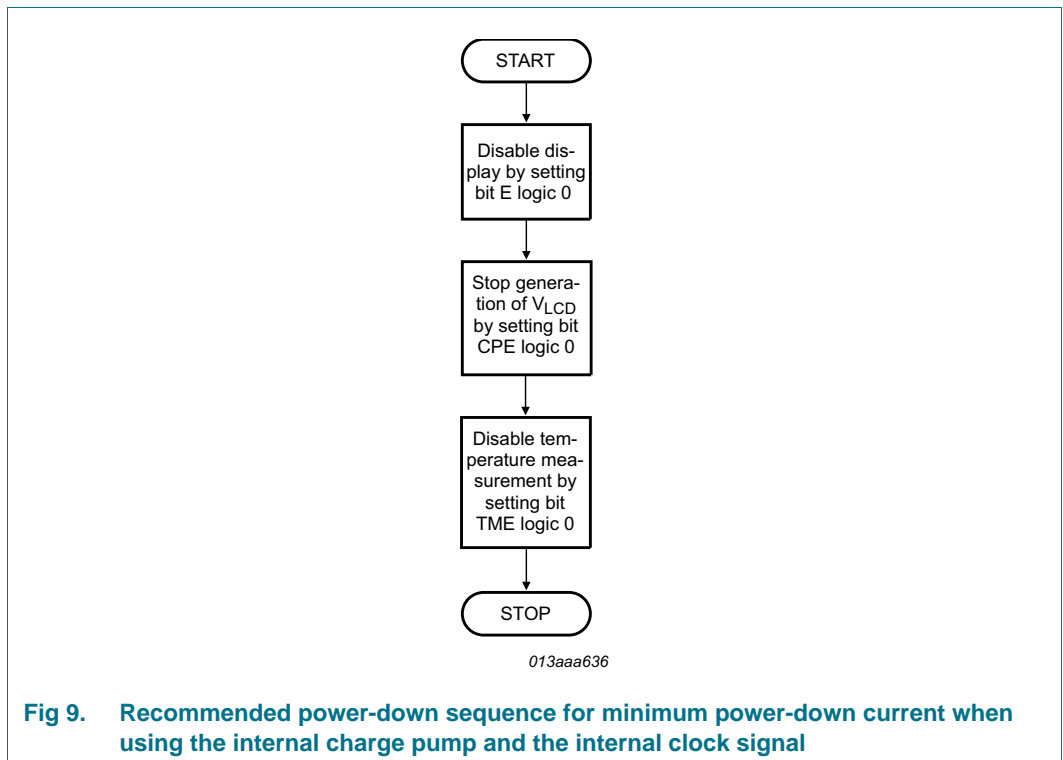
- (1) The external clock signal can be applied after the generation of the V_{LCD} voltage as well.
- (2) This time depends on the external capacitor on pin V_{LCD} . For a capacitor of 100 nF a delay of 5 ms to 15 ms is expected.

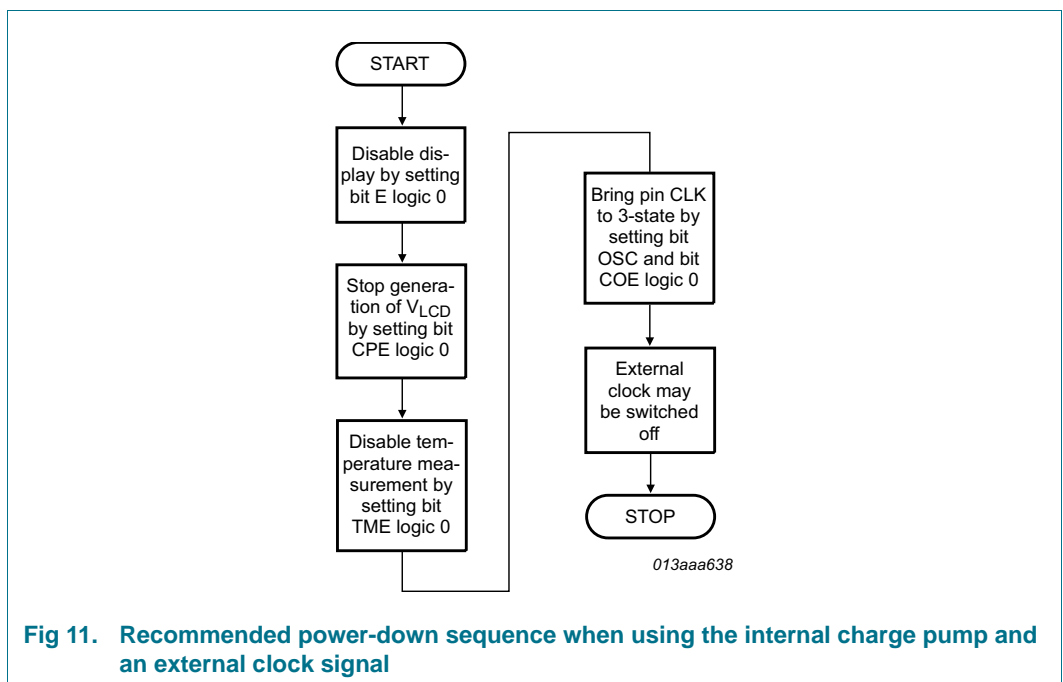
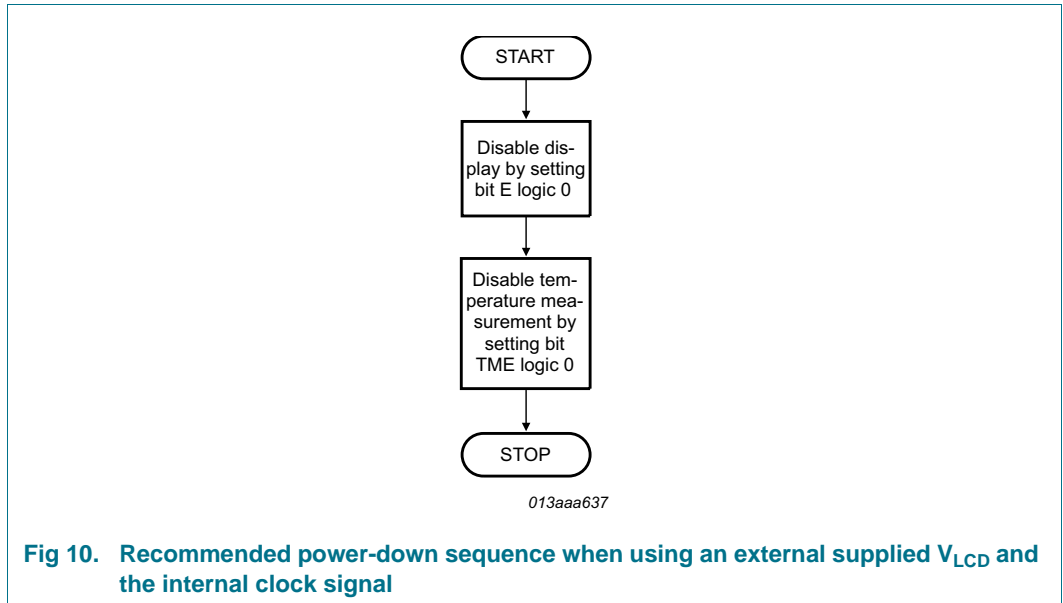
Fig 7. Recommended start-up sequence when using the internal charge pump and an external clock signal



8.2.4 Recommended sequences to enter power-down mode

With the following sequences, the PCA8537 can be set to a state of minimum power consumption, called power-down mode.





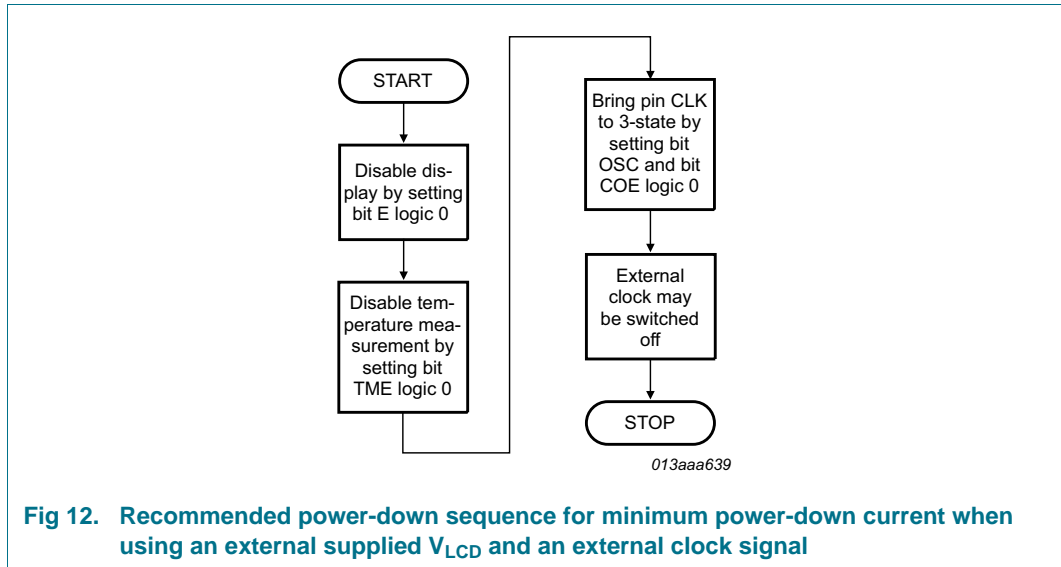


Fig 12. Recommended power-down sequence for minimum power-down current when using an external supplied V_{LCD} and an external clock signal

Remark: It is necessary to run the power-down sequence before removing the supplies. Depending on the application, care must be taken that no other signals are present at the chip input or output pins when removing the supplies (see [Section 10](#)). Otherwise this may cause unwanted display artifacts. In the case of uncontrolled removal of supply voltages the PCA8537 will not be damaged.

Remark: Static voltages across the liquid crystal display can build up when the external LCD supply voltage (V_{LCD}) is on while the IC supply voltage (V_{DD1} or V_{DD2}) is off, or the other way around. This may cause unwanted display artifacts. To avoid such artifacts, V_{LCD} , V_{DD1} , and V_{DD2} must be applied or removed together.

Remark: A clock signal must always be supplied to the device when the display is active. Removing the clock may freeze the LCD in a DC state, which is not suitable for the liquid crystal. It is recommended to first disable the display and afterwards to remove the clock signal.

8.3 Possible display configurations

The PCA8537 is a versatile peripheral device designed to interface between any microcontroller to a wide variety of LCD segment or dot matrix displays (see [Figure 13](#)). It can directly drive any static or multiplexed LCD containing up to eight backplanes with 44 segments.

The display configurations possible with the PCA8537 depend on the number of active backplane outputs required. A selection of possible display configurations is given in [Table 25](#).

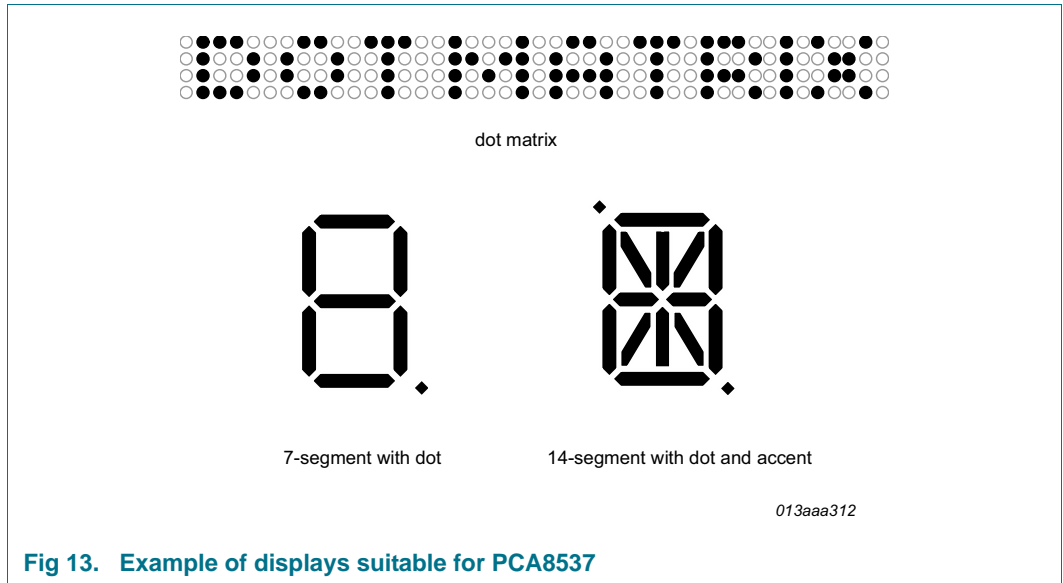


Fig 13. Example of displays suitable for PCA8537

Table 25. Selection of display configurations

| Number of | | | Digits/Characters | | Dot matrix/ Elements |
|------------|----------|-------|--------------------------|---------------------------|-------------------------|
| Backplanes | Segments | Icons | 7 segment ^[1] | 14 segment ^[2] | |
| 8 | 44 | 352 | 44 | 22 | 352 dots (8 × 44) |
| 6 | 46 | 276 | 34 | 17 | 276 dots (6 × 46) |
| 4 | 44 | 176 | 22 | 11 | 176 dots (4 × 44) |
| 2 | 44 | 88 | 11 | 5 | 88 dots (2 × 44) |
| 1 | 44 | 44 | 5 | 2 | 44 dots (1 × 44) |

[1] 7 segment display has 8 elements including the decimal point.

[2] 14 segment display has 16 elements including decimal point and accent dot.

All of the display configurations in Table 25 can be implemented in the typical systems shown in Figure 14 (internal V_{LCD}) and in Figure 15 (external V_{LCD}).

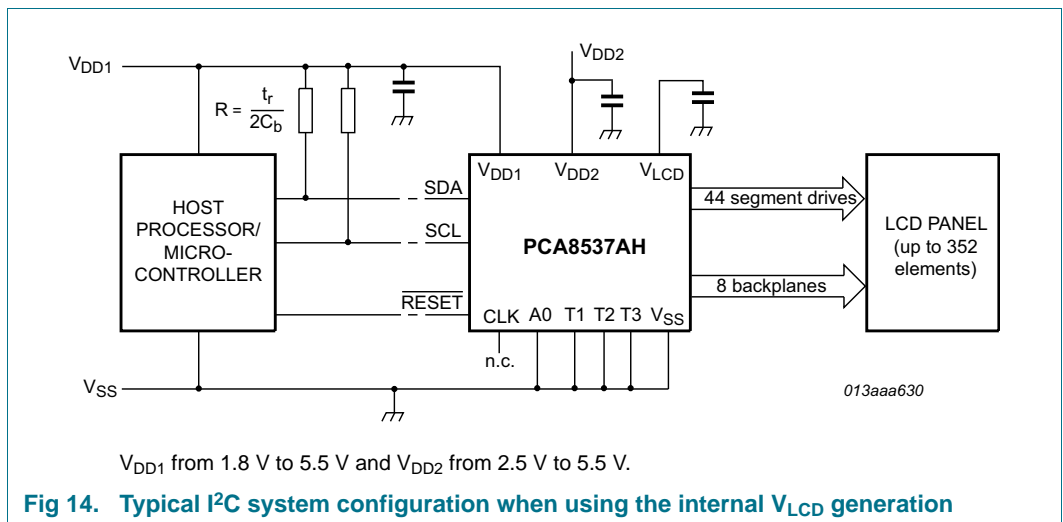
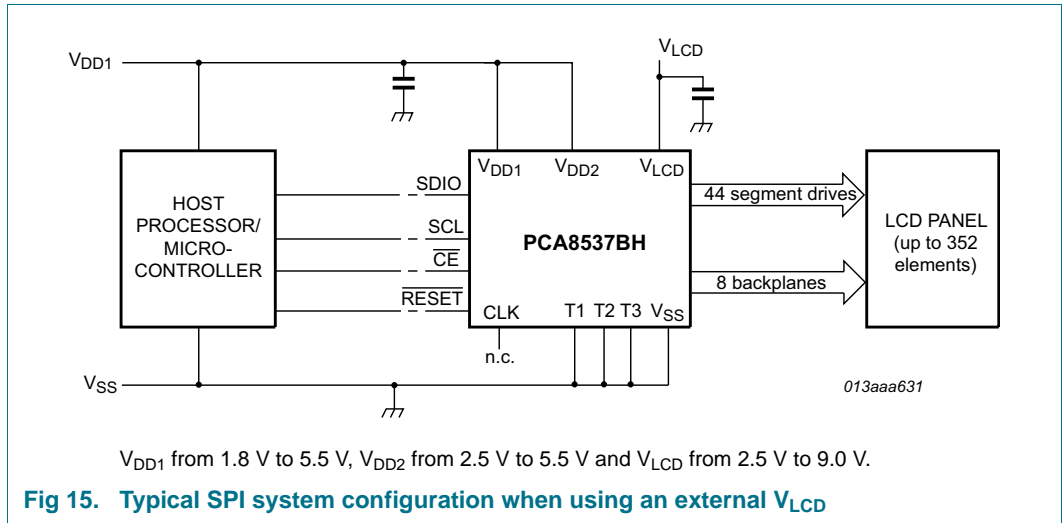


Fig 14. Typical I²C system configuration when using the internal V_{LCD} generation



The host microcontroller maintains the two-line I²C-bus communication channel with the PCA8537AH or the three-line SPI-bus with the PCA8537BH. The appropriate biasing voltages for the multiplexed LCD waveforms are generated internally. The only other connections required to complete the system are the power supplies (V_{DD1} , V_{DD2} , V_{SS} , V_{LCD}), the external capacitors, and the LCD panel selected for the application.

The recommended values for external capacitors on V_{DD1} , V_{DD2} , and V_{LCD} are of nominal 100 nF value. When using bigger capacitors, especially on the V_{LCD} , the generated ripple will be consequently smaller. However it will take longer for the internal charge pump to first reach the target V_{LCD} voltage.

If V_{DD1} and V_{DD2} are connected externally, the capacitors on V_{DD1} and V_{DD2} can be replaced by a single capacitor with a nominal value of 220 nF.

Remark: In case of insufficient decoupling, ripple on V_{DD1} and V_{DD2} will create additional V_{LCD} ripple. The ripple on the V_{LCD} can be reduced by making the V_{SS} connection as low-ohmic as possible. Excessive ripple on V_{LCD} may cause flicker on the display.

8.4 LCD supply voltage

8.4.1 External V_{LCD} supply

V_{LCD} can be directly supplied to the VLCD pin. In this case, the internal charge pump must not be enabled otherwise a high current may occur on pin VDD2 and pin VLCD. When V_{LCD} is supplied externally, no internal temperature compensation occurs on this voltage even if bit TCE is set logic 1 (see [Section 8.4.4.2](#)). The V_{LCD} voltage which is supplied externally will be available at the segments and backplanes of the device through the chosen bias system. Also programming VPR[7:0] will have no effect on the V_{LCD} which is externally supplied.

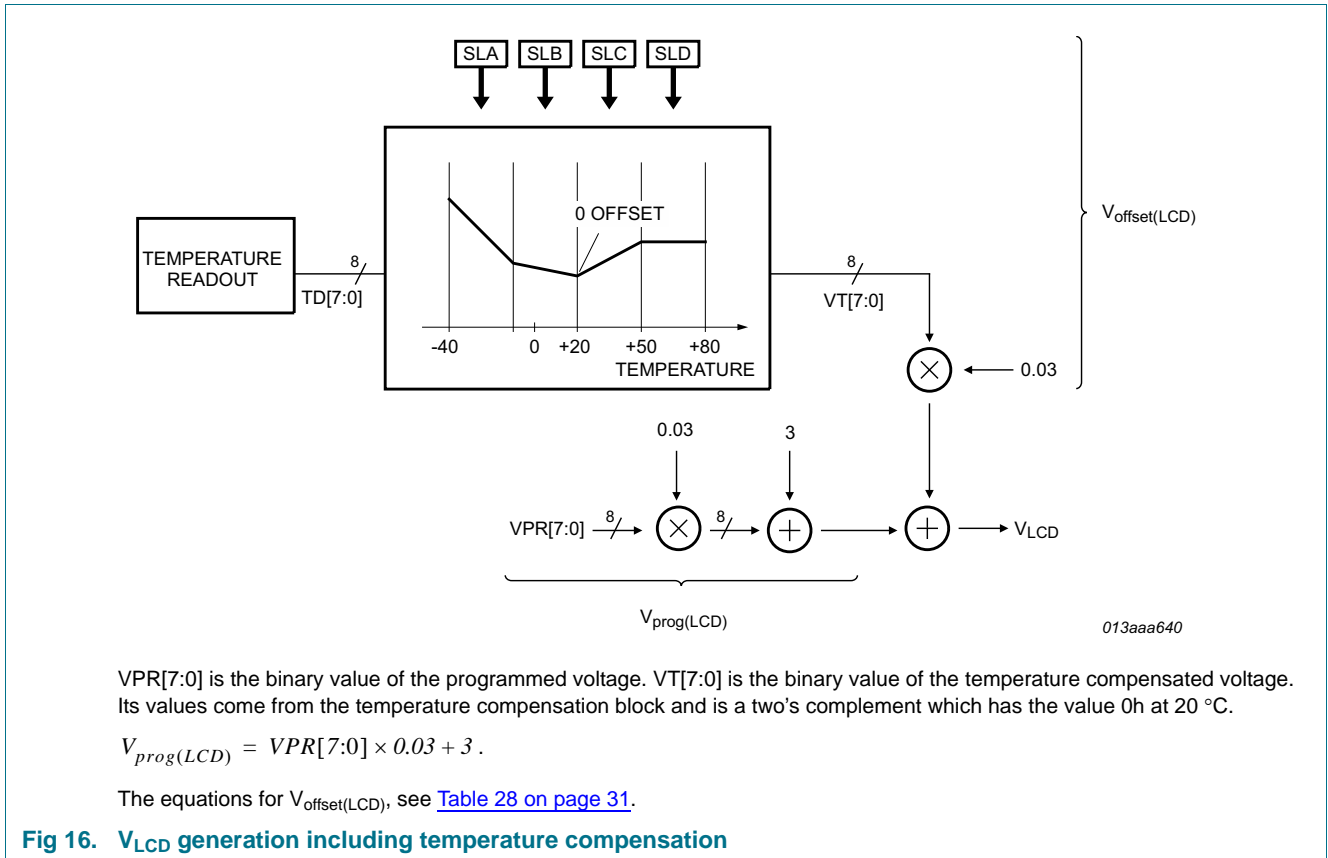
8.4.2 Internal V_{LCD} generation

V_{LCD} can be generated and controlled on the chip by using software commands. When the internal charge pump is used, the programmed V_{LCD} is available on pin VLCD. The charge pump generates a V_{LCD} of up to $3 \times V_{DD2}$. The charge pump can be enabled or disabled with the CPE bit (see [Table 9 on page 9](#)). With bit CPC, the charge pump multiplier setting can be configured.

The final value of V_{LCD} is a combination of the programmed $V_{prog(LCD)}$ value and the output of the temperature compensation block, $V_{offset(LCD)}$.

$$V_{LCD} = V_{prog(LCD)} + V_{offset(LCD)} \tag{1}$$

The system is shown in [Figure 16](#).



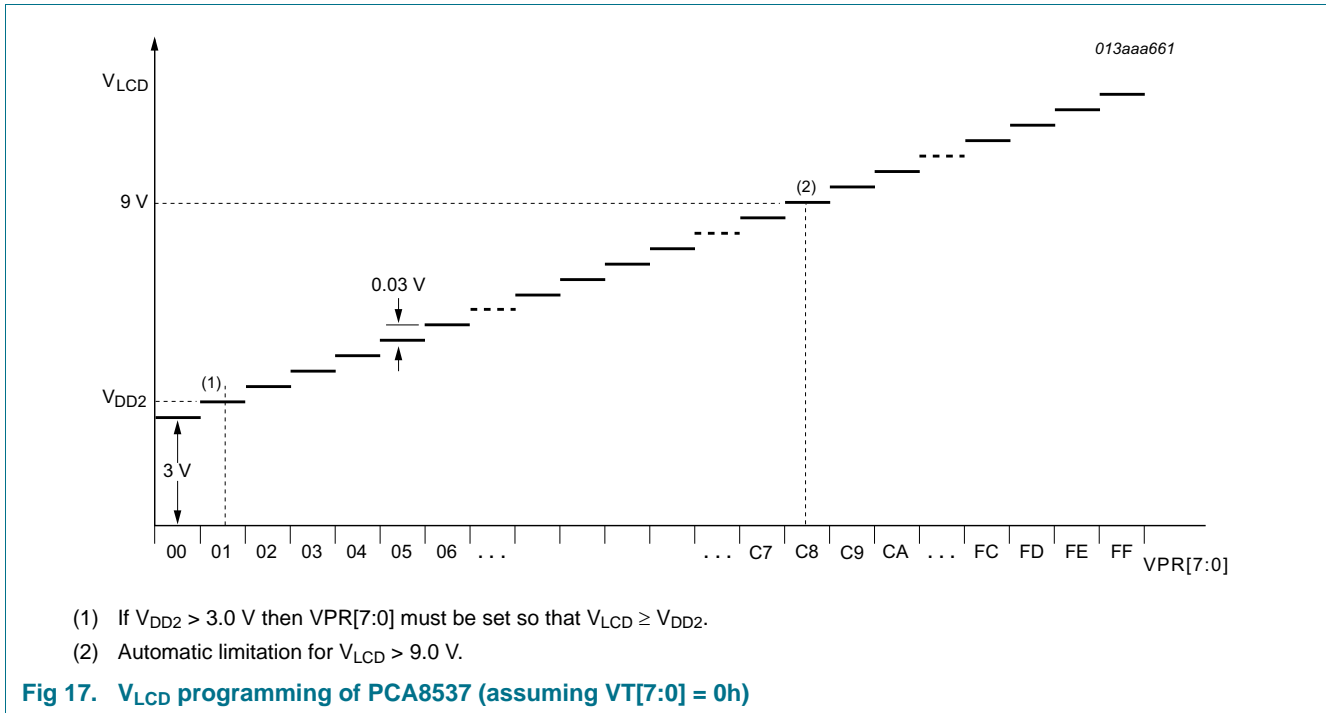
$VPR[7:0]$ is the binary value of the programmed voltage. $VT[7:0]$ is the binary value of the temperature compensated voltage. Its values come from the temperature compensation block and is a two's complement which has the value 0h at 20 °C.

$$V_{prog(LCD)} = VPR[7:0] \times 0.03 + 3.$$

The equations for $V_{offset(LCD)}$, see [Table 28 on page 31](#).

Fig 16. V_{LCD} generation including temperature compensation

[Figure 17](#) illustrates how V_{LCD} changes with the programmed value of $VPR[7:0]$.



The programmable range of $VPR[7:0]$ is from 0h to FFh. With the upper part of the programmable range, it is possible to achieve more than 9.0 V, but the PCA8537 has a built-in automatic limitation of V_{LCD} at 9.0 V. If V_{DD2} is higher than 3.0 V, then it is important that $VPR[7:0]$ is set to a value such that the resultant V_{LCD} (including the temperature correction of $VT[7:0]$) is higher than V_{DD2} .

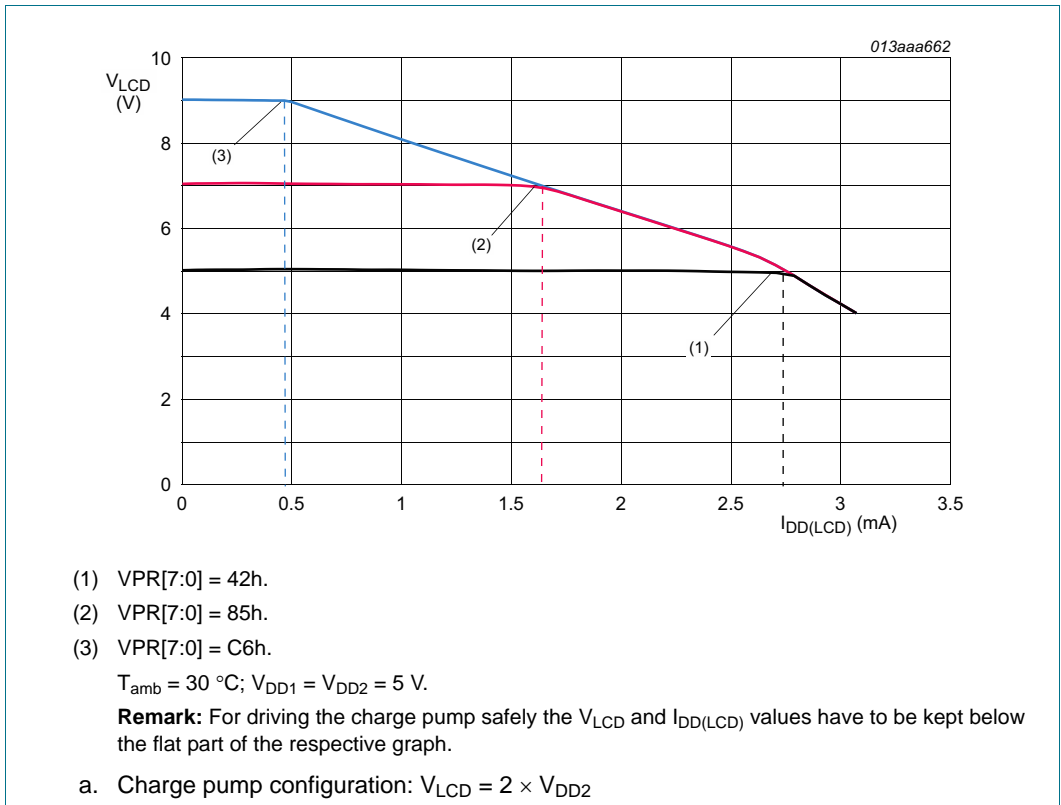
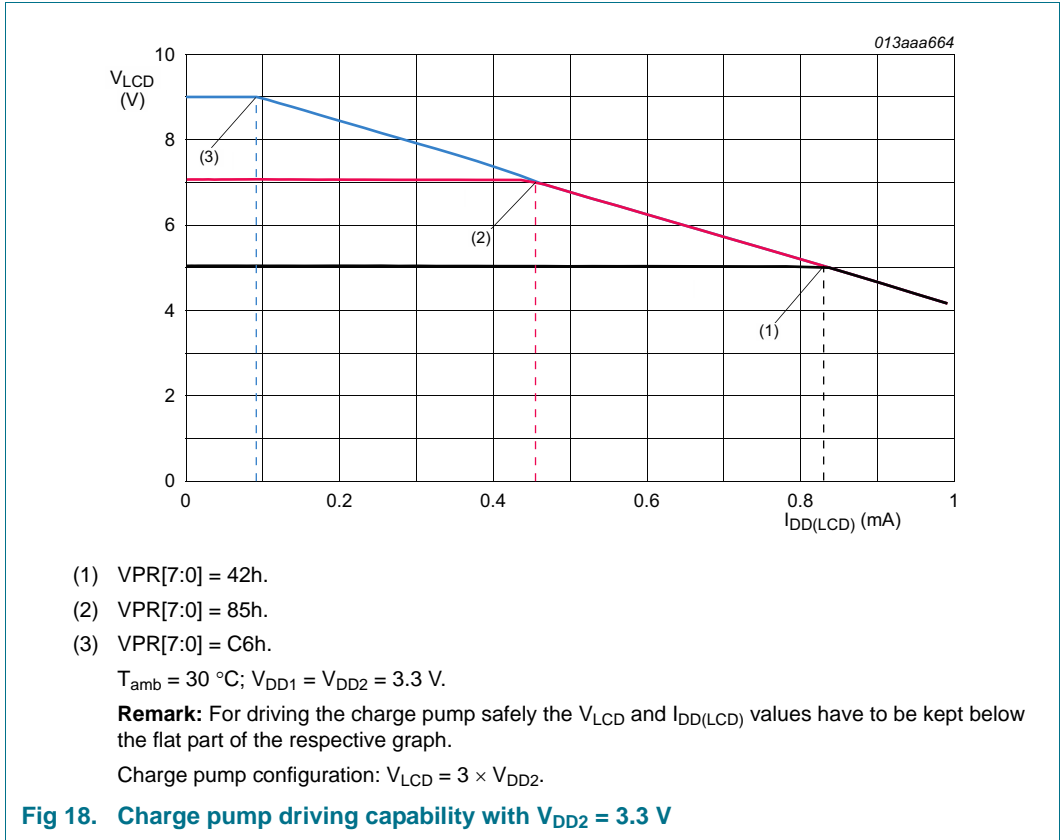
8.4.3 Charge pump

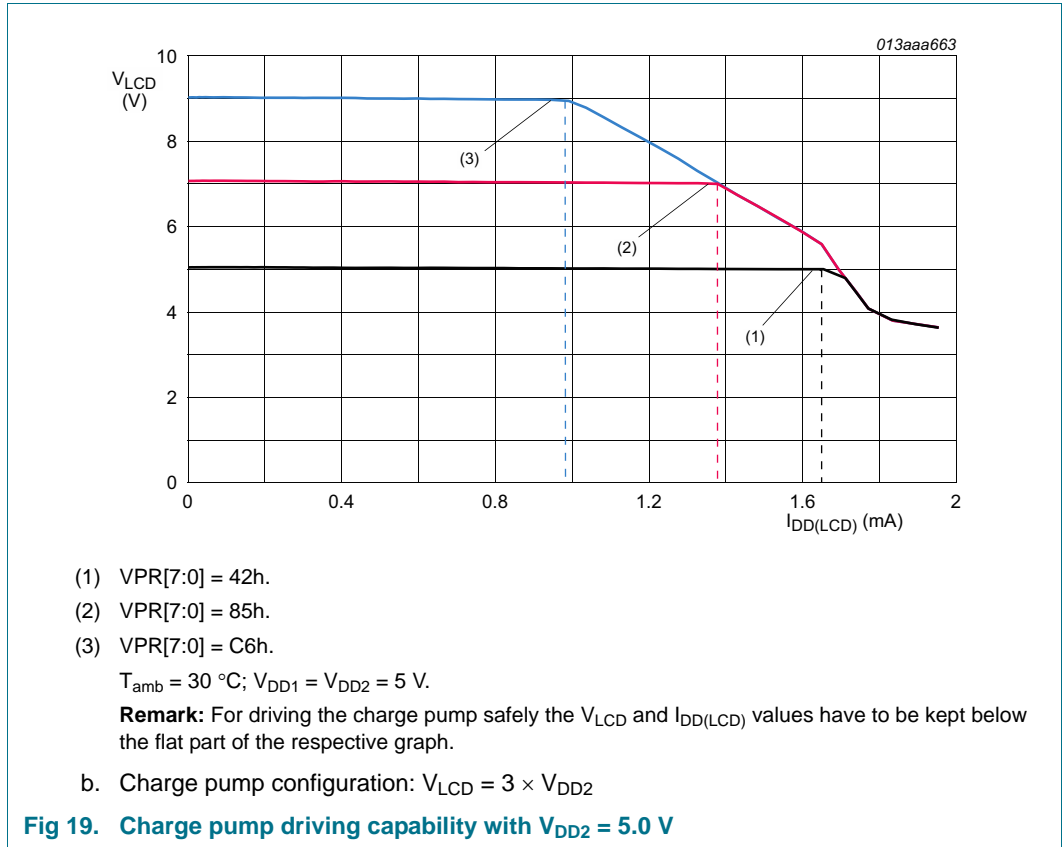
8.4.3.1 Charge pump configuration

To obtain the desired V_{LCD} values, the charge pump has to be configured properly. It has to be taken into account that the maximum theoretical values cannot be reached due to internal losses (see [Section 8.4.3.2](#)). So, for example, it is not possible to get a $V_{LCD} = 6.0\text{ V}$ with $V_{DD2} = 3.0\text{ V}$ and a charge pump configuration of 2 times V_{DD2} . In this case, a charge pump configuration of 3 times V_{DD2} is needed.

8.4.3.2 Charge pump driving capability

[Figure 18](#) and [Figure 19](#) are showing the charge pump driving capability with different settings of V_{DD2} and charge pump configurations.





8.4.4 Temperature measurement and temperature compensation of V_{LCD}

8.4.4.1 Temperature readout

The PCA8537 has a built-in temperature sensor which provides an 8 bit digital value, TD[7:0], of the ambient temperature. This value can be read through the interface (see [Figure 47 on page 54](#) and [Figure 51 on page 57](#)). The actual temperature is determined from TD[7:0] using [Equation 2](#):

$$T\text{ (}^{\circ}\text{C)} = 0.9375 \times TD[7:0] - 40 \tag{2}$$

The measurement needs about 5 ms to complete and is repeated periodically as soon as bit TME is set logic 1 (see [Table 10 on page 10](#)). The time between measurements is linked to the system clock and hence varies with changes in the chosen frame frequency, see [Table 26](#).

Table 26. Temperature measurement update rate

| Selected frame frequency | Temperature measurement update rate |
|--------------------------|-------------------------------------|
| 60 Hz | 3.3 s |
| 200 Hz | 1 s |
| 300 Hz | 0.67 s |

The temperature sensor can be thought of as analog to digital converter. Like all A/D converters, jitter will exist on the LSB of the output value. This is also true of the temperature sensor in the PCA8537. Jitter of the LSB of TD[7:0] may lead to contrast

stepping of the display due to the V_{LCD} voltage is periodically changing between two different target voltages. For this reason, a filter has been implemented to ensure that LSB jitter does not affect the display performance.

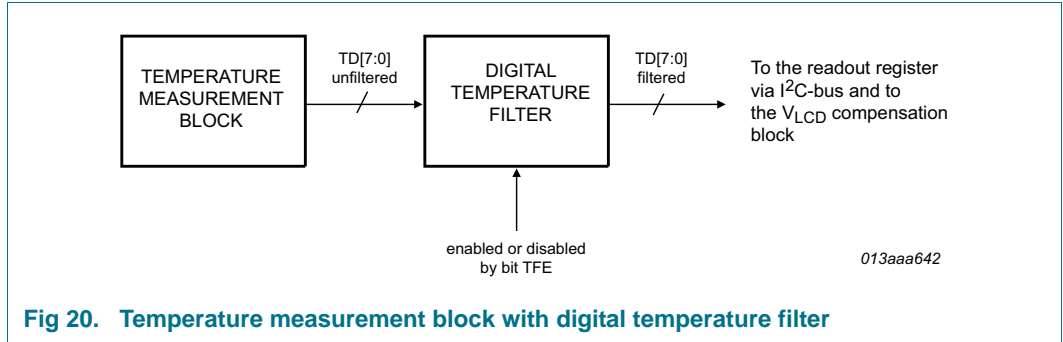
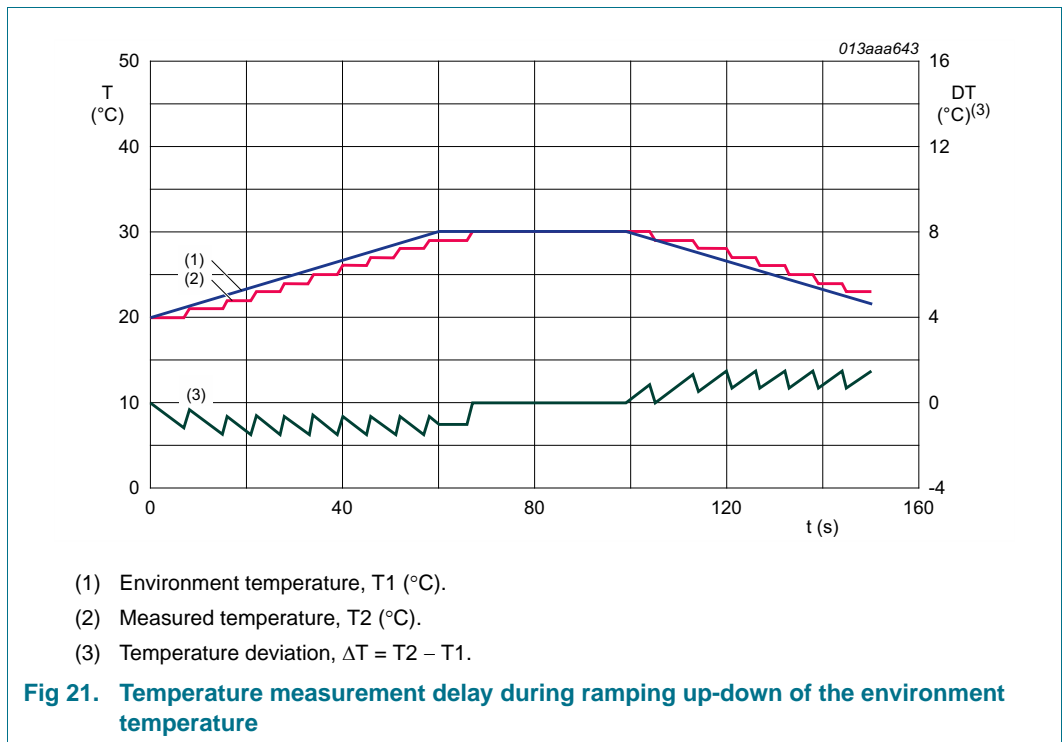


Fig 20. Temperature measurement block with digital temperature filter

Like any other filtering, the digital temperature filter (see Figure 20) introduces a certain delay in the measurement of temperature. This behavior is illustrated in Figure 21.



- (1) Environment temperature, T_1 (°C).
- (2) Measured temperature, T_2 (°C).
- (3) Temperature deviation, $\Delta T = T_2 - T_1$.

Fig 21. Temperature measurement delay during ramping up-down of the environment temperature

This delay may cause undesired effects at start-up when the environment temperature may be different than the reset value of the PCA8537 which is 20 °C. In this case, it takes up to 30 s until the correct measured temperature value will be available. A control bit, TFE (see Table 23 on page 16), is implemented to enable or disable the digital temperature filter. This bit is set logic 0 by default, which means, that the filter is disabled and the unfiltered environment temperature value is available to calculate the desired V_{LCD} .

8.4.4.2 Temperature adjustment of the V_{LCD}

Due to the temperature dependency of the liquid crystal viscosity the LCD controlling voltage V_{LCD} might have to be adjusted at different temperatures to maintain optimal contrast. The temperature behavior of the liquid comes from the LCD manufacturer. The slope has to be set to compensate for the liquid behavior. Internal temperature compensation may be enabled via bit TCE (see [Table 10 on page 10](#)).

The ambient temperature range is split up into four equally sized regions and a different temperature coefficient can be applied to each. Each coefficient can be selected from a choice of eight different slopes. Each one of these coefficients may be independently selected (see [Table 27](#)).

Table 27. Temperature coefficients

| SLA to SLD register value | Corresponding slope factor, SFA to SFD (mV/°C) |
|---------------------------|--|
| 000 ^[1] | 0 |
| 001 | -4 |
| 010 | -8 |
| 011 | -16 |
| 100 | -40 |
| 101 | +4 |
| 110 | +8 |
| 111 | +16 |

[1] Default value.

The slope factors imply a linear correction, however the implementation is in steps of 30 mV.

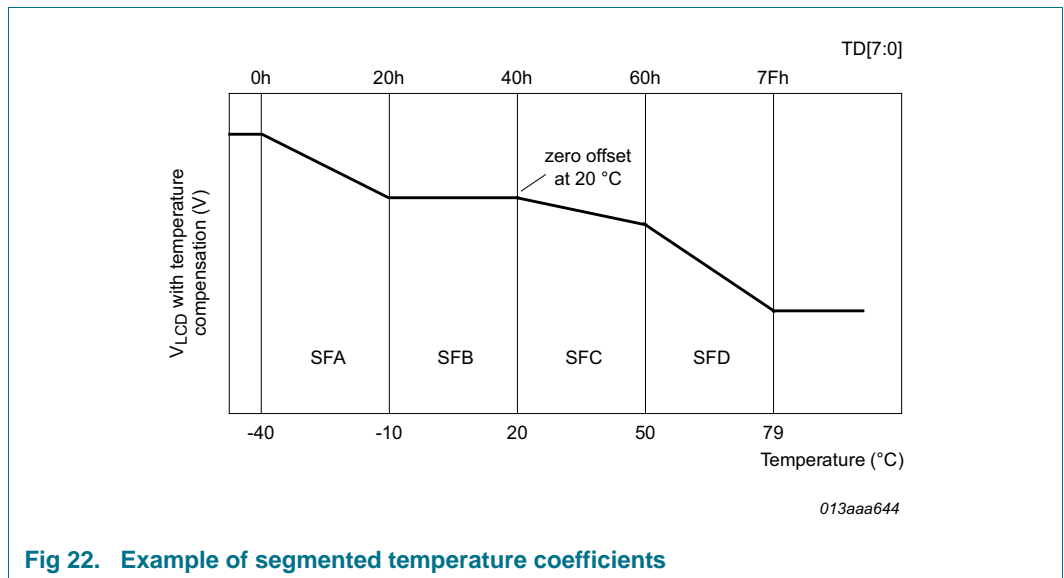


Fig 22. Example of segmented temperature coefficients

The offset voltage is calculated according to [Table 28](#).

Table 28. Calculation of the V_{LCD} offset voltage

| Temperature range | V _{offset(LCD)} voltage (mV) |
|--------------------------|--|
| T ≤ -40 °C | $V_{offset(LCD)} = 30 \times SFA + 30 \times SFB$ |
| -40 °C ≤ T ≤ -10 °C | $V_{offset(LCD)} = (-10 - T) \times SFA + 30 \times SFB$ |
| -10 °C < T ≤ 20 °C | $V_{offset(LCD)} = (20 - T) \times SFB$ |
| 20 °C < T ≤ 50 °C | $V_{offset(LCD)} = (T - 20) \times SFC$ |
| 50 °C < T < 80 °C | $V_{offset(LCD)} = (T - 50) \times SFD + 30 \times SFC$ |
| 80 °C ≤ T ^[1] | $V_{offset(LCD)} = 30 \times SFD + 30 \times SFC$ |

[1] No temperature compensation is possible above 80 °C. Above this value, the system maintains the compensation value from 80 °C.

Example: Assumed that T_{amb} = -8 °C; SFB= -16 mV/°C:

$$V_{offset(LCD)} = (20 - -8) \times (-16) = 28 \times (-16) = -448mV$$

Remark: Care must be taken that the ranges of VPR[7:0] and VT[7:0] do not cause clipping and hence undesired results. The device will not permit overflow or underflow and will clamp results to either end of the range.

8.4.5 LCD voltage selector

The LCD voltage selector co-ordinates the multiplexing of the LCD in accordance with the selected LCD drive configuration. The operation of the voltage selector is controlled by the Set-bias-mode command (see [Table 15 on page 12](#)) and the Set-MUX-mode command (see [Table 14 on page 12](#)).

Intermediate LCD biasing voltages are obtained from an internal voltage divider. The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of V_{LCD} and the resulting discrimination ratios (D), are given in [Table 29](#).

Discrimination is a term which is defined as the ratio of the one and off RMS voltage across a segment. It can be thought of as a measurement of contrast.

Table 29. LCD drive modes: summary of characteristics

| LCD drive mode | Number of: | | LCD bias configuration | $\frac{V_{off(RMS)}}{V_{LCD}}$ | $\frac{V_{on(RMS)}}{V_{LCD}}$ | $D = \frac{V_{on(RMS)}}{V_{off(RMS)}}$ [1] | V_{LCD} [2] |
|-------------------|------------|-------------|------------------------|--------------------------------|-------------------------------|--|---------------------|
| | Backplanes | Bias levels | | | | | |
| static | 1 | 2 | static | 0 | 1 | ∞ | $V_{on(RMS)}$ |
| 1:2 multiplex | 2 | 3 | $\frac{1}{2}$ | 0.354 | 0.791 | 2.236 | $2.828V_{off(RMS)}$ |
| 1:2 multiplex | 2 | 4 | $\frac{1}{3}$ | 0.333 | 0.745 | 2.236 | $3.0V_{off(RMS)}$ |
| 1:2 multiplex [3] | 2 | 5 | $\frac{1}{4}$ | 0.395 | 0.729 | 1.845 | $2.529V_{off(RMS)}$ |
| 1:4 multiplex [3] | 4 | 3 | $\frac{1}{2}$ | 0.433 | 0.661 | 1.527 | $2.309V_{off(RMS)}$ |
| 1:4 multiplex | 4 | 4 | $\frac{1}{3}$ | 0.333 | 0.577 | 1.732 | $3.0V_{off(RMS)}$ |
| 1:4 multiplex [3] | 4 | 5 | $\frac{1}{4}$ | 0.331 | 0.545 | 1.646 | $3.024V_{off(RMS)}$ |
| 1:6 multiplex [3] | 6 | 3 | $\frac{1}{2}$ | 0.456 | 0.612 | 1.341 | $2.191V_{off(RMS)}$ |
| 1:6 multiplex | 6 | 4 | $\frac{1}{3}$ | 0.333 | 0.509 | 1.527 | $3.0V_{off(RMS)}$ |
| 1:6 multiplex | 6 | 5 | $\frac{1}{4}$ | 0.306 | 0.467 | 1.527 | $3.266V_{off(RMS)}$ |
| 1:8 multiplex [3] | 8 | 3 | $\frac{1}{2}$ | 0.467 | 0.586 | 1.254 | $2.138V_{off(RMS)}$ |
| 1:8 multiplex [3] | 8 | 4 | $\frac{1}{3}$ | 0.333 | 0.471 | 1.414 | $3.0V_{off(RMS)}$ |
| 1:8 multiplex | 8 | 5 | $\frac{1}{4}$ | 0.293 | 0.424 | 1.447 | $3.411V_{off(RMS)}$ |

[1] Determined from Equation 5.

[2] Determined from Equation 4.

[3] In these examples, the discrimination factor and hence the contrast ratios are smaller. The advantage of these LCD drive modes is a power saving from a reduction of the LCD voltage V_{LCD} .

A practical value for V_{LCD} is determined by equating $V_{off(RMS)}$ with a defined LCD threshold voltage (V_{th}), typically when the LCD exhibits approximately 10 % contrast. In the static drive mode, a suitable choice is $V_{LCD} > 3V_{th}$.

Bias is calculated by $\frac{1}{1+a}$, where the values for a are

a = 1 for $\frac{1}{2}$ bias

a = 2 for $\frac{1}{3}$ bias

a = 3 for $\frac{1}{4}$ bias

The RMS on-state voltage ($V_{on(RMS)}$) for the LCD is calculated with Equation 3

$$V_{on(RMS)} = V_{LCD} \sqrt{\frac{a^2 + 2a + n}{n \times (1 + a)^2}} \tag{3}$$

where V_{LCD} is the resultant voltage at the LCD segment and where the values for n are

n = 1 for static mode

n = 2 for 1:2 multiplex

n = 4 for 1:4 multiplex

n = 6 for 1:6 multiplex

n = 8 for 1:8 multiplex

The RMS off-state voltage ($V_{off(RMS)}$) for the LCD is calculated with Equation 4:

$$V_{off(RMS)} = V_{LCD} \sqrt{\frac{a^2 - 2a + n}{n \times (1 + a)^2}} \tag{4}$$

Discrimination is the ratio of $V_{on(RMS)}$ to $V_{off(RMS)}$ and is determined from [Equation 5](#):

$$\frac{V_{on(RMS)}}{V_{off(RMS)}} = \sqrt{\frac{(a + 1)^2 + (n - 1)}{(a - 1)^2 + (n - 1)}} \tag{5}$$

It should be noted that V_{LCD} is sometimes referred as the LCD operating voltage.

8.4.5.1 Electro-optical performance

Suitable values for $V_{on(RMS)}$ and $V_{off(RMS)}$ are dependent on the LCD liquid used. The RMS voltage, at which a pixel will be switched on or off, determine the transmissibility of the pixel.

For any given liquid, there are two threshold values defined. One point is at 10 % relative transmission (at $V_{th(off)}$) and the other at 90 % relative transmission (at $V_{th(on)}$), see [Figure 23](#). For a good contrast performance, the following rules should be followed:

$$V_{on(RMS)} \geq V_{th(on)} \tag{6}$$

$$V_{off(RMS)} \leq V_{th(off)} \tag{7}$$

$V_{on(RMS)}$ and $V_{off(RMS)}$ are properties of the display driver and are affected by the selection of a (see [Equation 3](#)), n (see [Equation 5](#)), and the V_{LCD} voltage.

$V_{th(off)}$ and $V_{th(on)}$ are properties of the LCD liquid and can be provided by the module manufacturer. $V_{th(off)}$ is sometimes just named V_{th} . $V_{th(on)}$ is sometimes named saturation voltage V_{sat} .

It is important to match the module properties to those of the driver in order to achieve optimum performance.

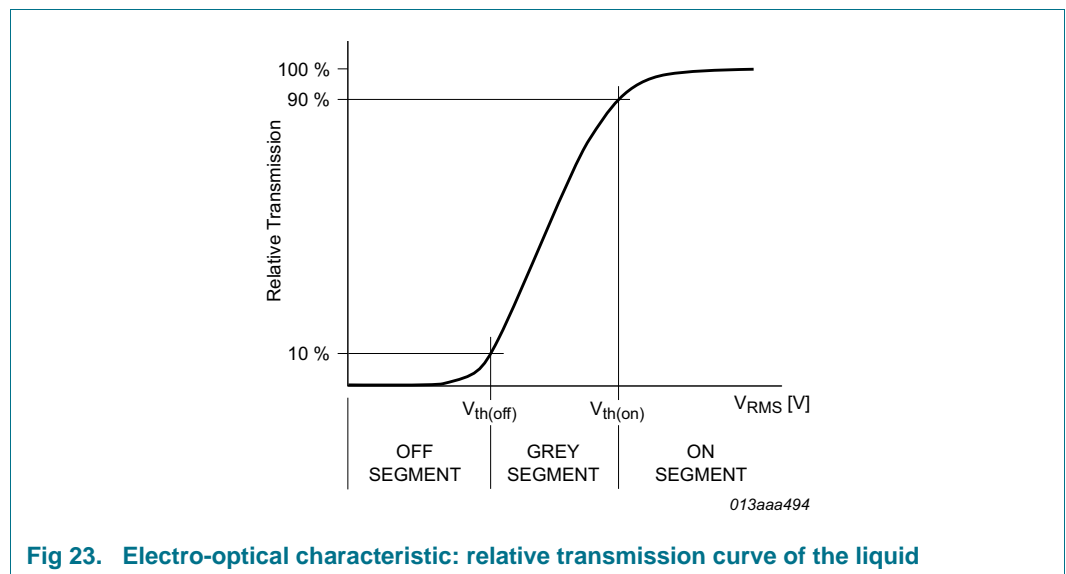
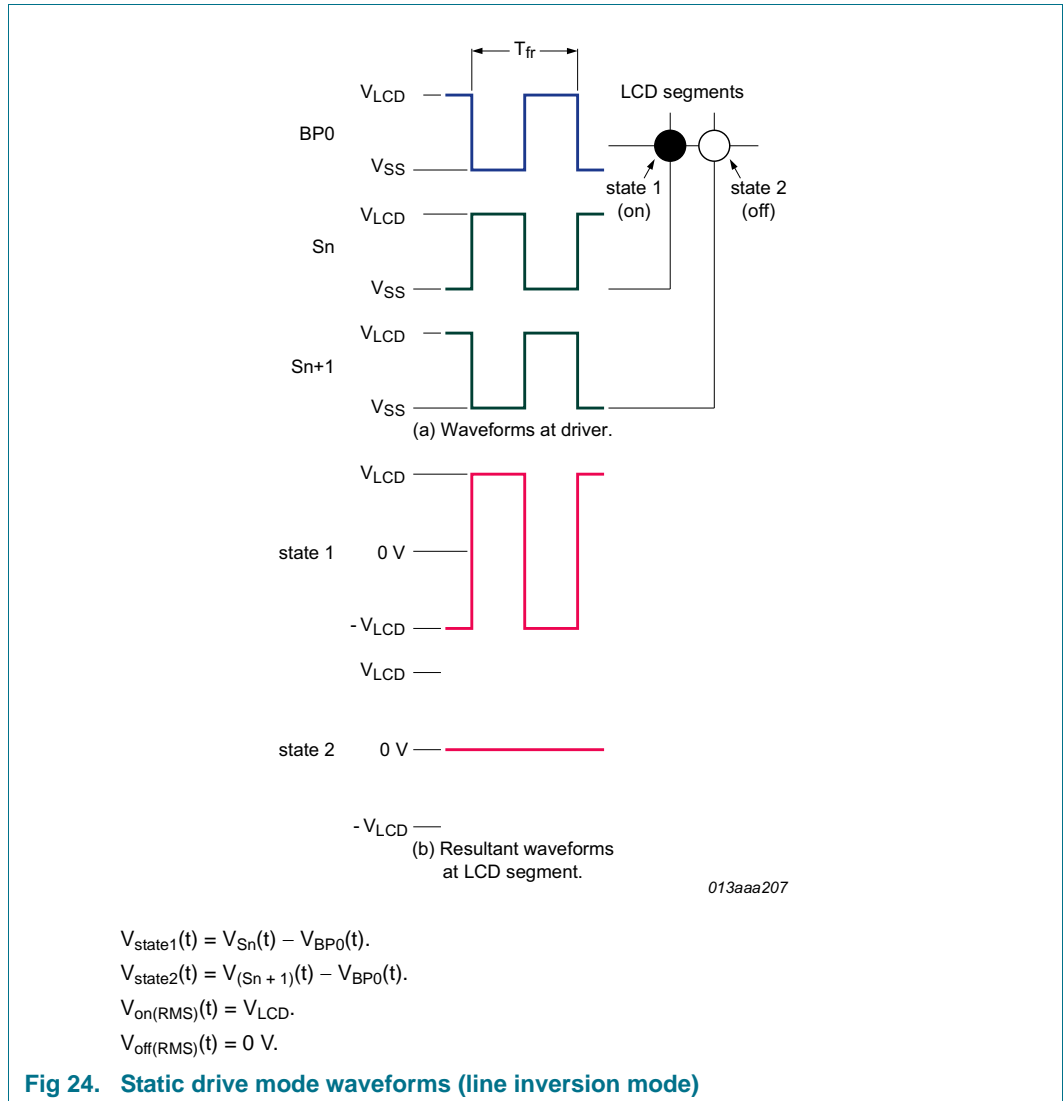


Fig 23. Electro-optical characteristic: relative transmission curve of the liquid

8.4.6 LCD drive mode waveforms

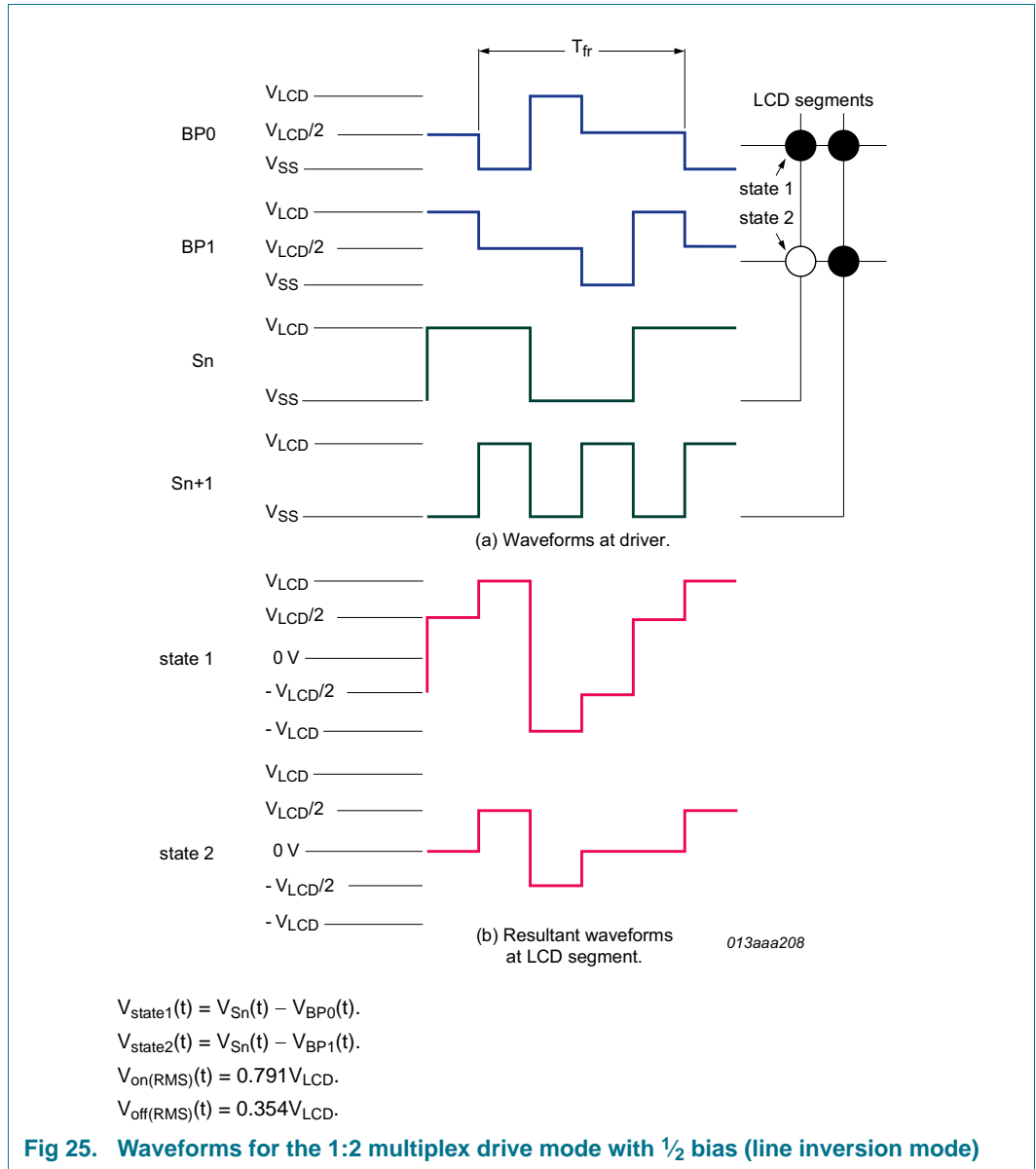
8.4.6.1 Static drive mode

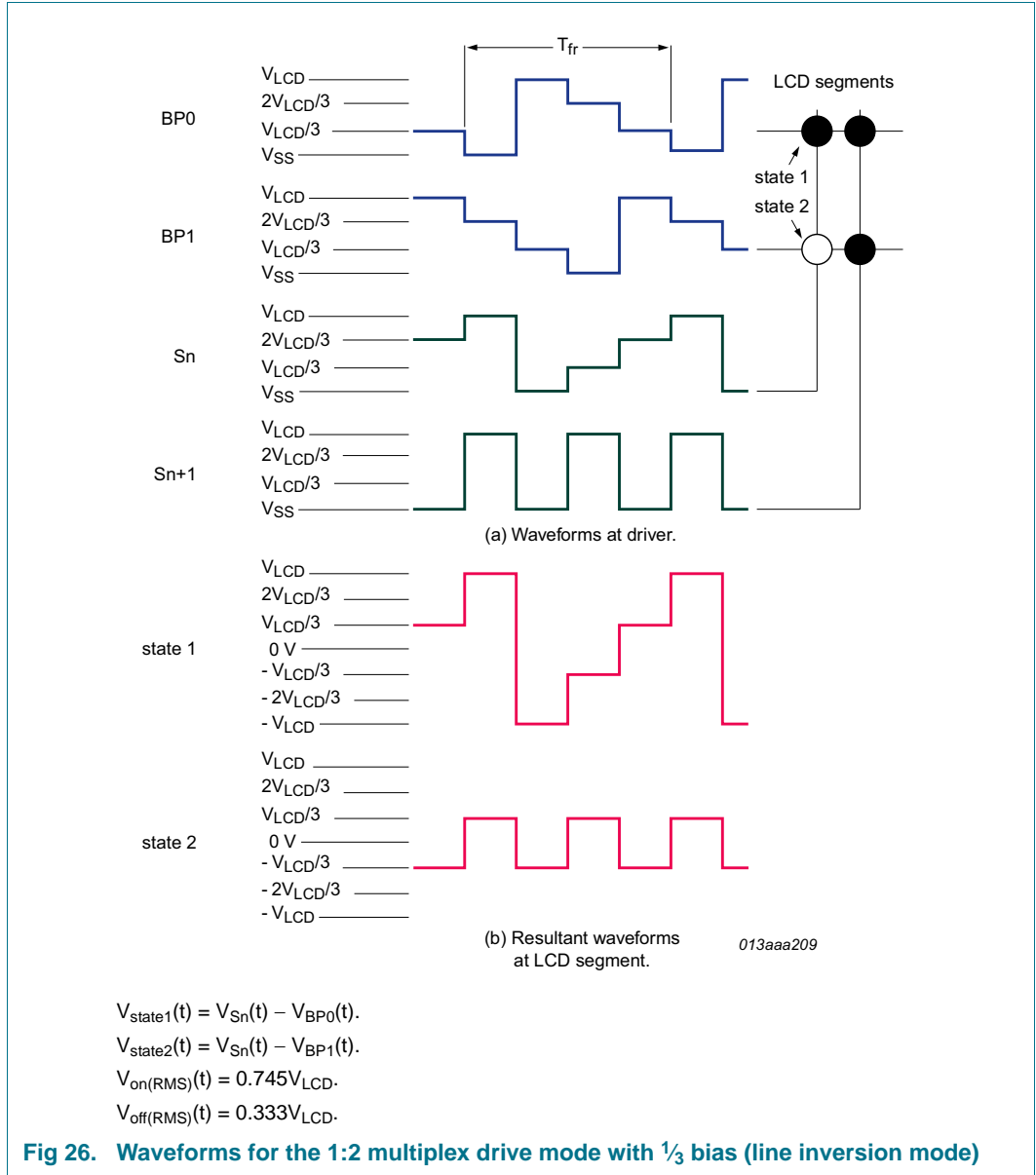
The static LCD drive mode is used when a single backplane is provided in the LCD.



8.4.6.2 1:2 multiplex drive mode

When two backplanes are provided in the LCD, the 1:2 multiplex mode applies. The PCA8537 allows the use of 1/2 bias or 1/3 bias in this mode as shown in Figure 25 and Figure 26.





8.4.6.3 1:4 multiplex drive mode

When four backplanes are provided in the LCD, the 1:4 multiplex drive mode applies, as shown in Figure 27.

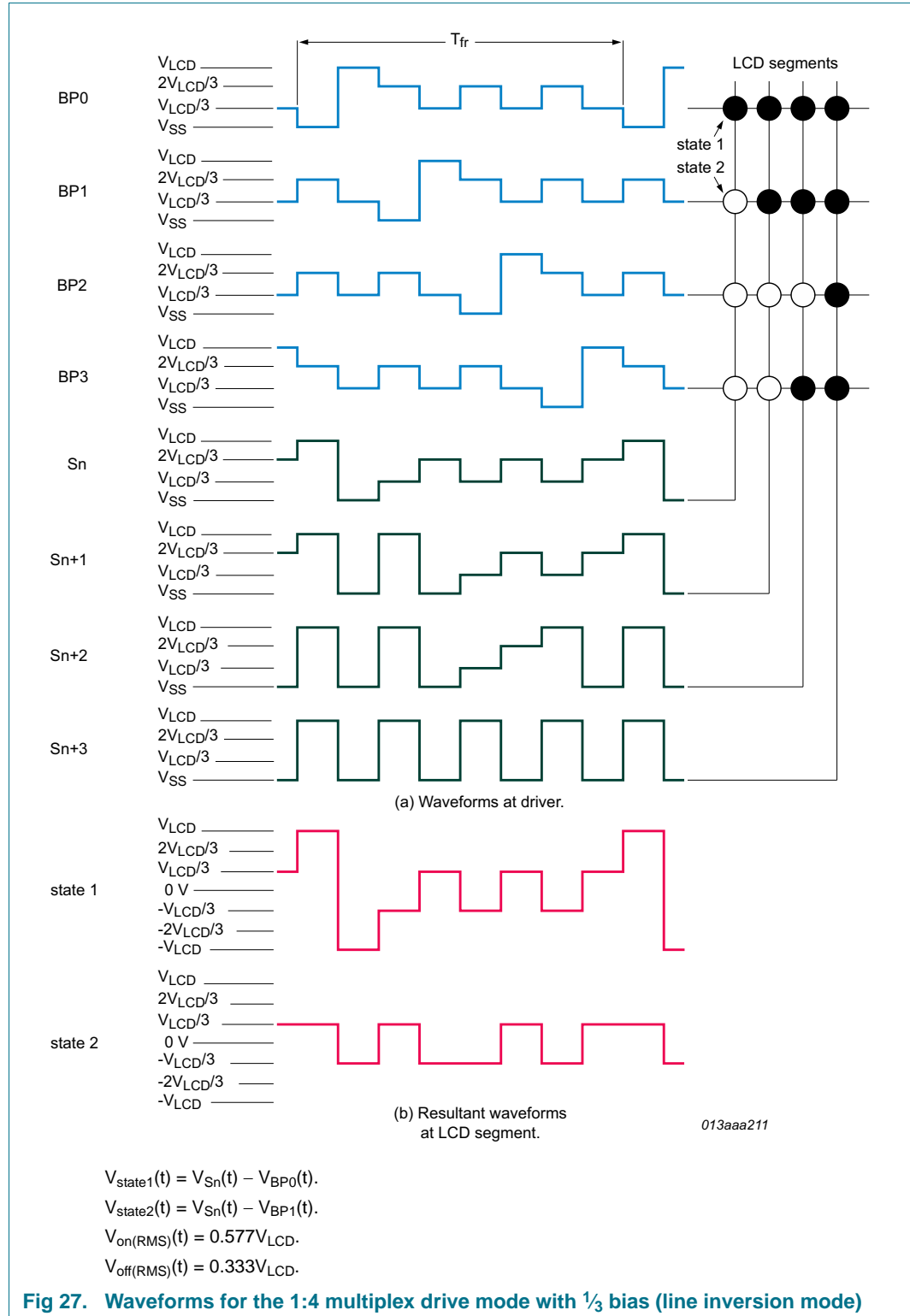
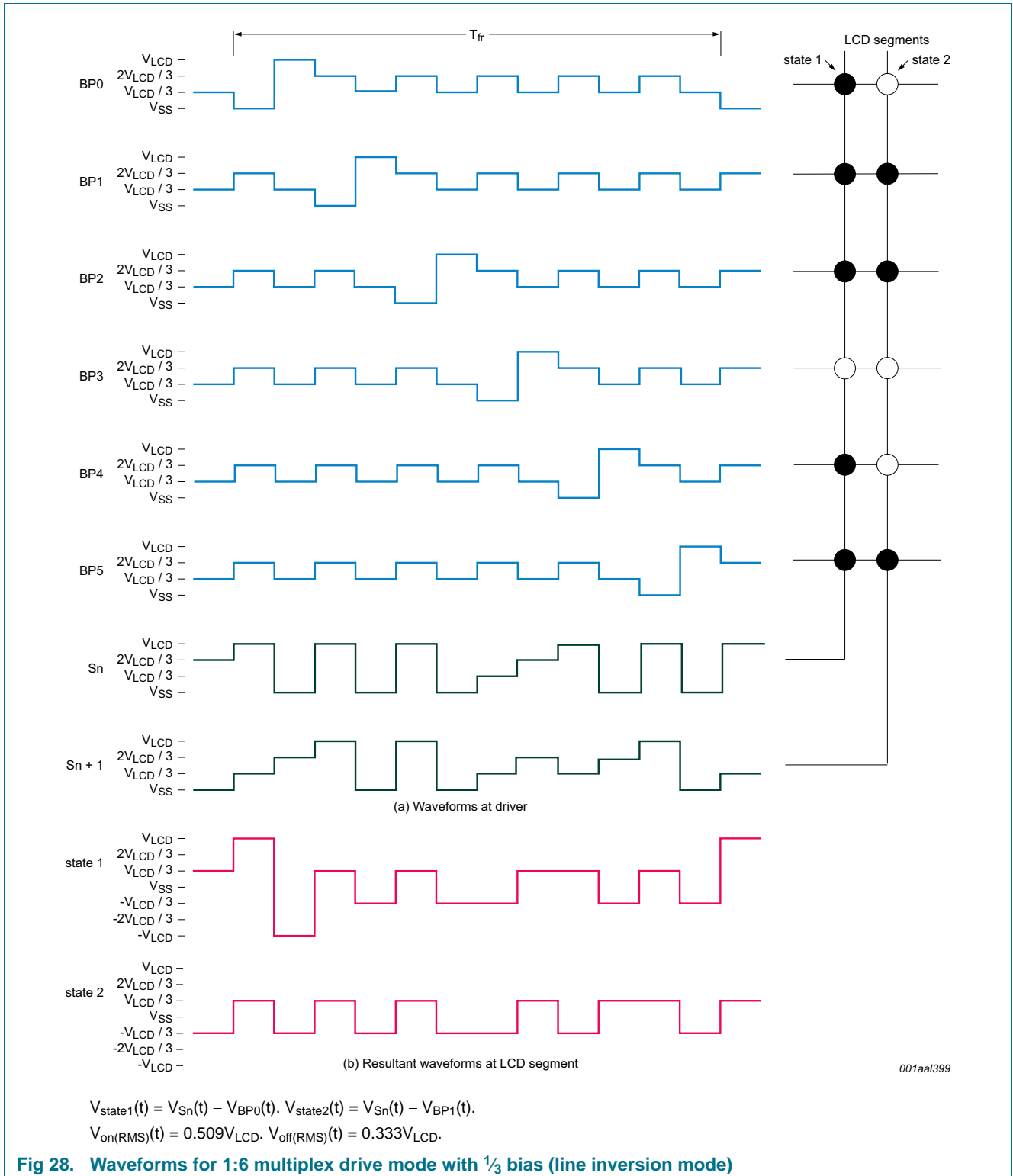
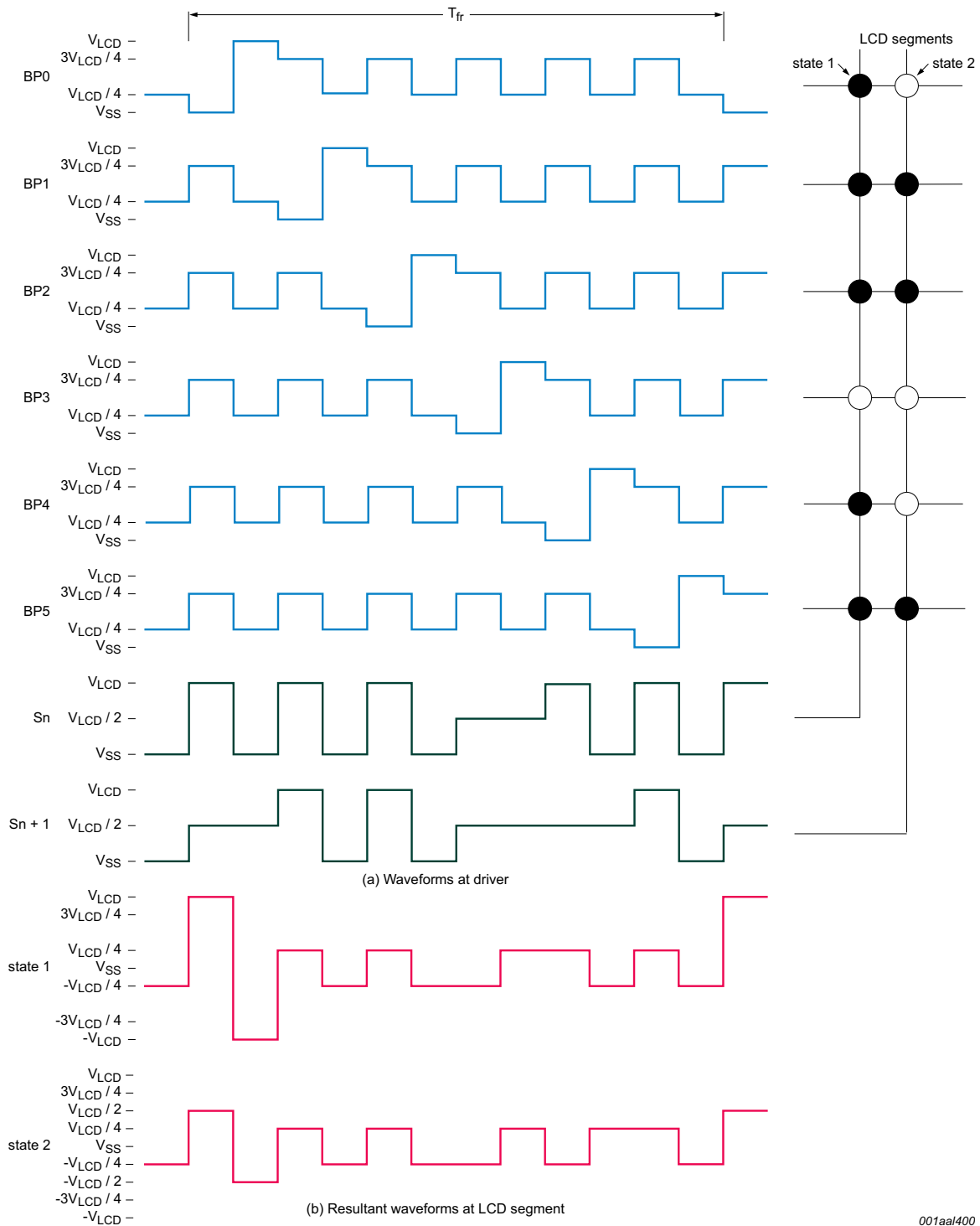


Fig 27. Waveforms for the 1:4 multiplex drive mode with 1/3 bias (line inversion mode)

8.4.6.4 1:6 multiplex drive mode

When six backplanes are provided in the LCD, the 1:6 multiplex drive mode applies. The PCA8537 allows the use of $\frac{1}{3}$ bias or $\frac{1}{4}$ bias in this mode as shown in [Figure 28](#) and [Figure 29](#).





$$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t). \quad V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t).$$

$$V_{on(RMS)}(t) = 0.467V_{LCD}. \quad V_{off(RMS)}(t) = 0.306V_{LCD}.$$

Fig 29. Waveforms for 1:6 multiplex drive mode with 1/4 bias (line inversion mode)

001aal400

8.4.6.5 1:8 multiplex drive mode

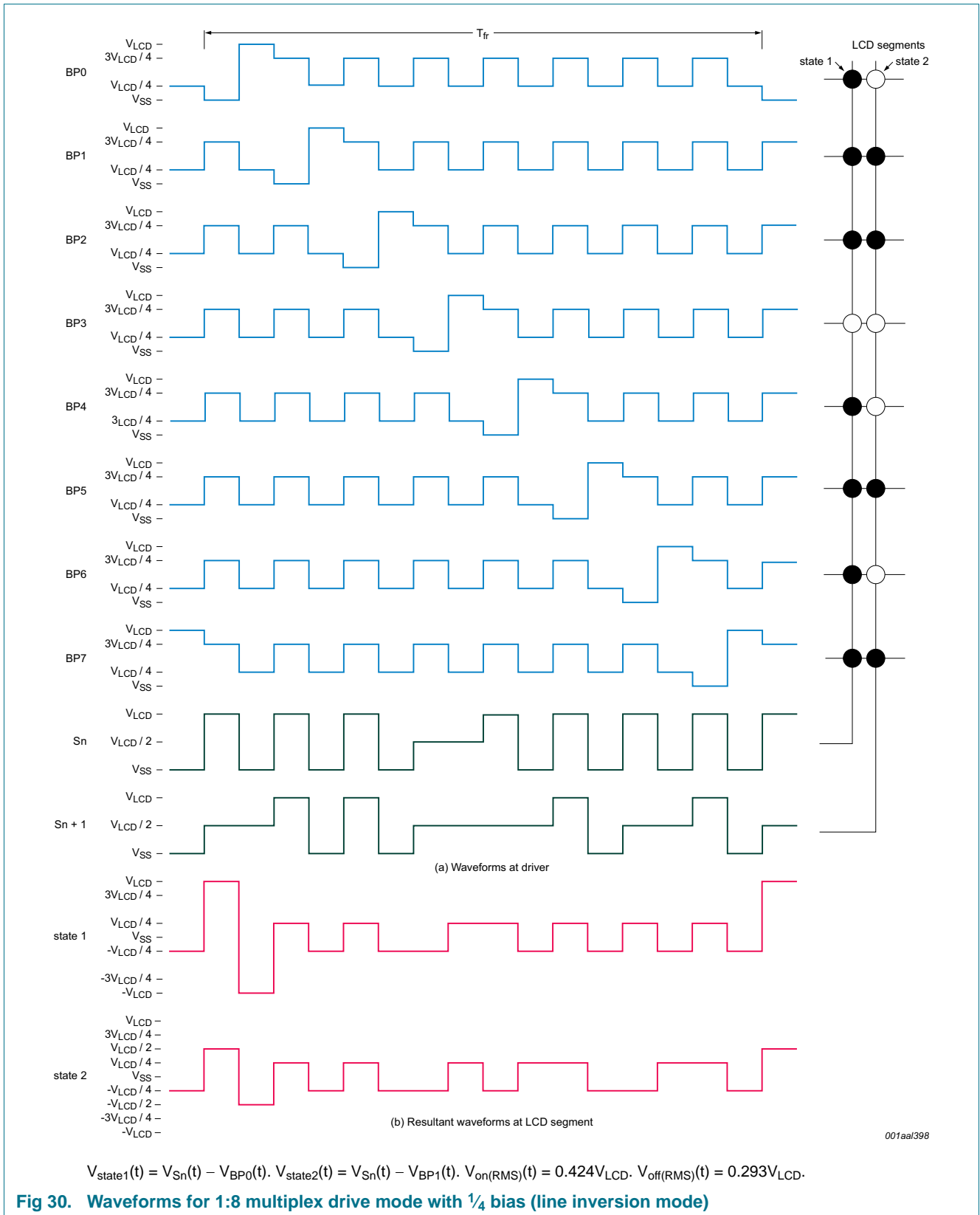
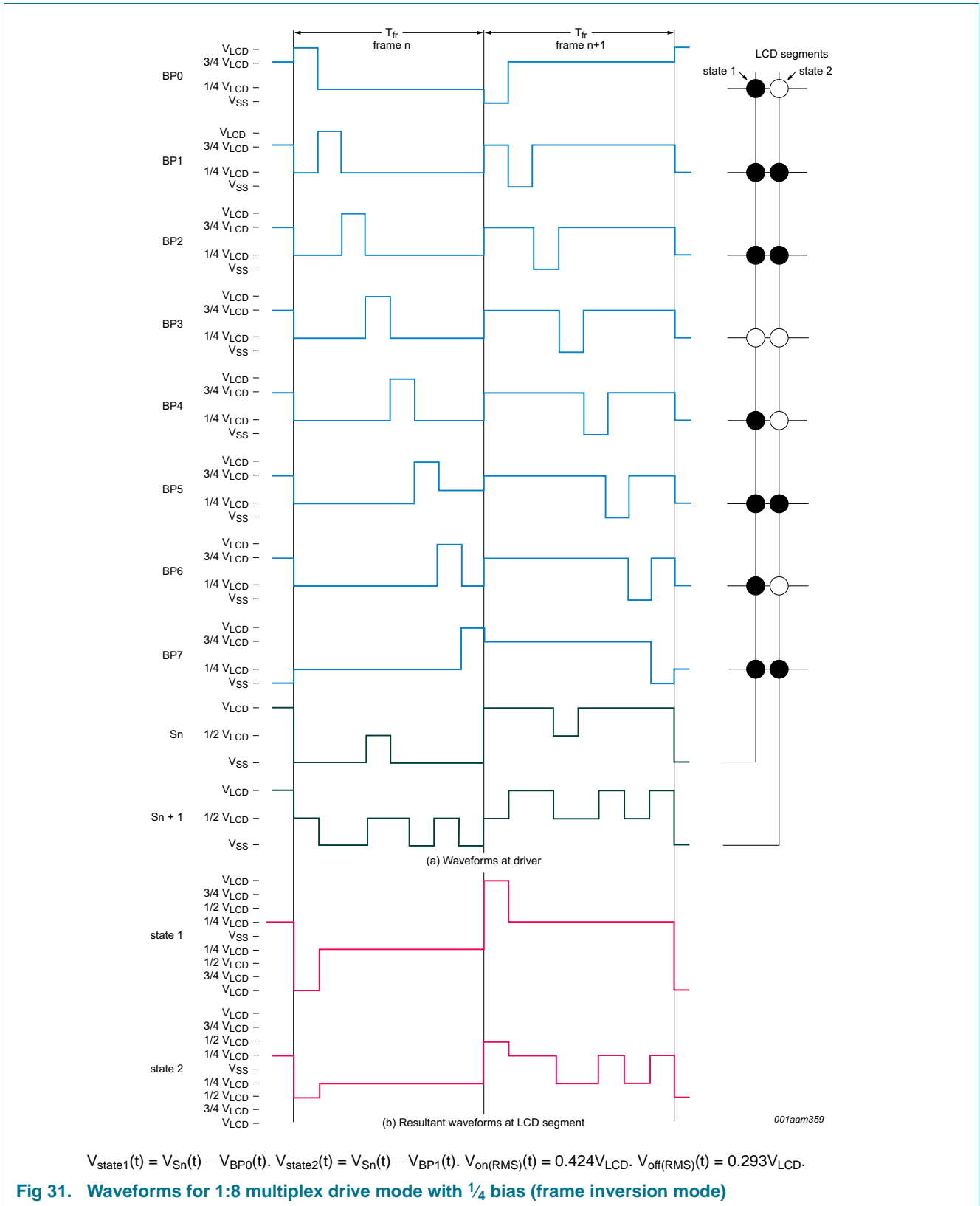


Fig 30. Waveforms for 1:8 multiplex drive mode with 1/4 bias (line inversion mode)



8.5 Backplane and segment outputs

8.5.1 Backplane outputs

The LCD drive section includes eight backplane outputs: BP0 to BP7. The backplane output signals are generated based on the selected LCD multiplex drive mode.

[Table 30](#) describes which outputs are active for each of the multiplex drive modes and what signal is generated.

Table 30. Mapping of output pins and corresponding signals with respect to driving mode

| MUX mode | Output pin | | | | | | | |
|----------|------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|
| | BP0 | BP1 | BP2 | BP3 | BP4 | BP5 | S45/BP6 | S44/BP7 |
| | Signal | | | | | | | |
| 1:8 | BP0 | BP1 | BP2 | BP3 | BP4 | BP5 | BP6 | BP7 |
| 1:6 | BP0 | BP1 | BP2 | BP3 | BP4 | BP5 | S45 | S44 |
| 1:4 | BP0 | BP1 | BP2 | BP3 | BP0 ^[1] | BP1 ^[1] | BP2 ^[1] | BP3 ^[1] |
| 1:2 | BP0 | BP1 | BP0 ^[1] | BP1 ^[1] | BP0 ^[1] | BP1 ^[1] | BP0 ^[1] | BP1 ^[1] |
| static | BP0 | BP0 ^[1] | BP0 ^[1] | BP0 ^[1] | BP0 ^[1] | BP0 ^[1] | BP0 ^[1] | BP0 ^[1] |

[1] These pins may optionally or alternatively be connected to the display to improve drive strength. Connect only with the corresponding output pin carrying the same signal. If not required, they can be left open circuit.

8.5.1.1 1:8 multiplex drive mode

In 1:8 multiplex drive mode, BP0 to BP7 must be connected directly to the LCD.

8.5.1.2 1:6 multiplex drive mode

1:6 multiplex mode is a special case. In this mode BP0 to BP5 must be connected directly to the display as back plane signals and S44 and S45 must be connected to the display as segment signals.

8.5.1.3 1:4 multiplex drive mode

In the 1:4 multiplex drive mode, BP0 to BP3 must be connected directly to the LCD.

The unused BPs may be left open-circuit. Optionally they may also be connected to the display to increase drive strength.

- BP0 is repeated on BP4
- BP1 is repeated on BP5
- BP2 is repeated on BP6
- BP3 is repeated on BP7

8.5.1.4 1:2 multiplex drive mode

In the 1:2 multiplex drive mode, BP0 and BP1 must be connected directly to the LCD.

The unused BPs may be left open-circuit. Optionally they may also be connected to the display to increase drive strength.

- BP0 is repeated on BP2, BP4, and BP6
- BP1 is repeated on BP3, BP5, and BP7

8.5.1.5 Static drive mode

In the static drive mode, BP0 must be connected directly to the LCD.

In the static drive mode, the same signal is carried by all eight backplane outputs and they can be connected in parallel for very high drive requirements.

- BP0 is repeated on BP1, BP2, BP3, BP4, BP5, BP6, and BP7

8.5.2 Segment outputs

The LCD drive section includes up to 46 segment outputs. Segments S0 to S43 are always segment outputs. There are also two more segment outputs which become active in 1:6 multiplex mode. These are S45/BP6 and S44/BP7 and must also be connected directly to the display.

The segment output signals are generated based on the multiplexed backplane signals and with data resident in the display register. When less than 46 segment outputs are required, the unused segment outputs must be left open-circuit.

8.5.2.1 Static, 1:8, 1:4, 1:2 multiplex drive mode

In these drive modes, segments S0 to S43 must be connected to the display.

8.5.2.2 1:6 multiplex drive mode

In this drive mode, segments S0 to S43, S44, and S45 must be connected to the display.

8.6 Display controller

The display controller executes the commands identified by the command decoder. It contains the status registers of the PCA8537 and co-ordinates their effects. The controller is also responsible for loading display data into the display RAM as required by the filling order.

8.7 Display register

The display register holds the display data while the corresponding multiplex signals are generated.

8.8 Display RAM

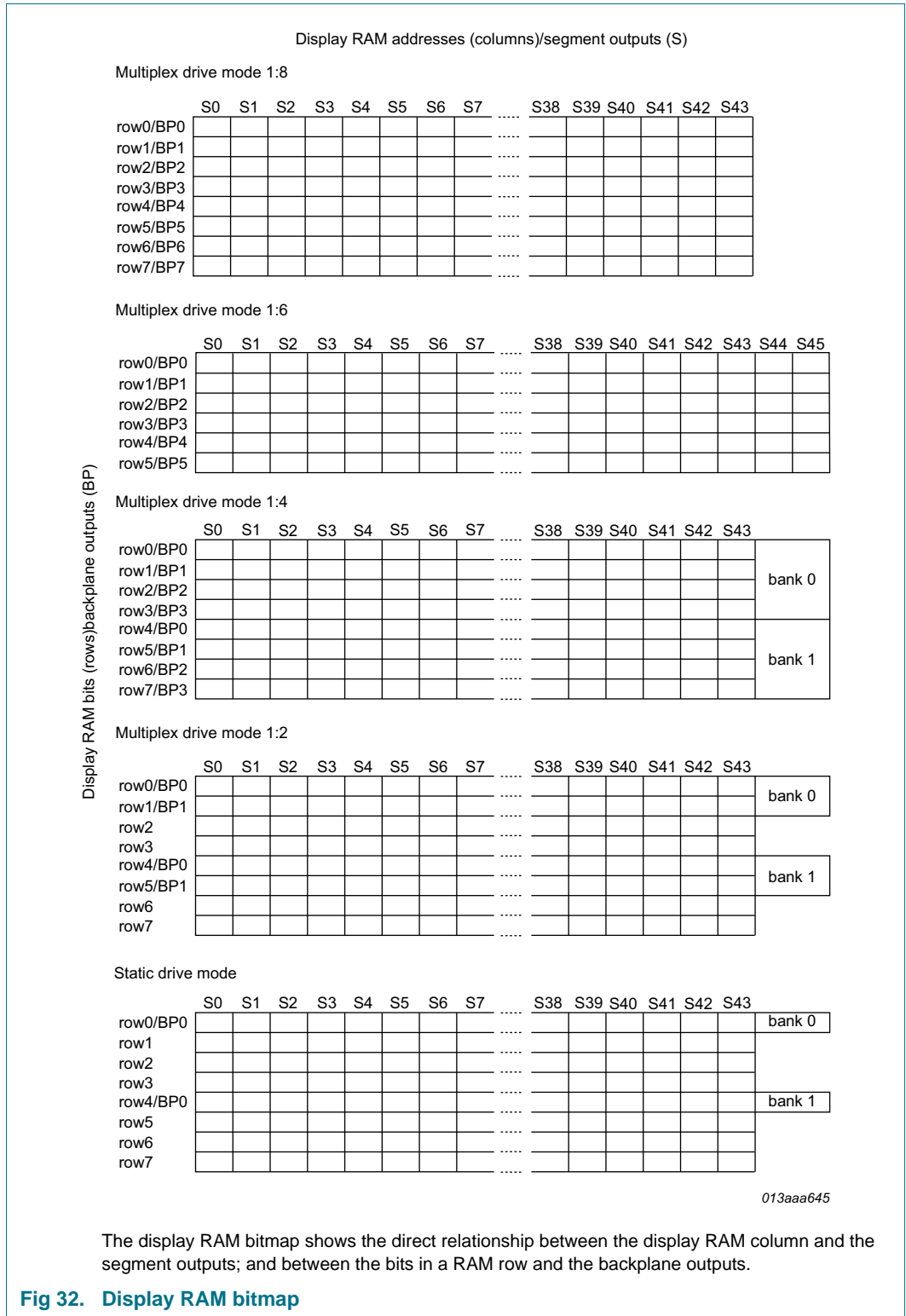
The display RAM stores LCD data. Depending on the multiplex drive mode, the arrangement of the RAM is changed.

- multiplex drive mode 1:8: RAM is 44 × 8 bit
- multiplex drive mode 1:6: RAM is 46 × 6 bit
- multiplex drive mode 1:4: RAM is 44 × 4 bit arranged in two banks
- multiplex drive mode 1:2: RAM is 44 × 2 bit arranged in two banks
- static drive mode: RAM is 44 × 1 bit arranged in two banks

A logic 1 in the RAM bit map indicates the on-state of the corresponding LCD element; similarly, a logic 0 indicates the off-state.

There is a one-to-one correspondence between

- the bits in the RAM bitmap and the LCD elements,
- the RAM columns and the segment outputs,
- the RAM rows and the backplane outputs.



The display RAM bit map, [Figure 32](#), shows row 0 to row 7 which correspond with the backplane outputs BP0 to BP7, and column 0 to column 45 which correspond with the segment outputs S0 to S45. In multiplexed LCD applications, the data of each row of the display RAM is time-multiplexed with the corresponding backplane (row 0 with BP0, row 1 with BP1, and so on).

When display data is transmitted to the PCA8537, the display bytes received are stored in the display RAM in accordance with the selected LCD multiplex drive mode. The data is stored as it arrives. Depending on the current multiplex drive mode, data is stored singularly, in pairs, quadruples, sextuples or bytes.

8.8.1 Data pointer

The addressing mechanism for the display RAM is realized using the data pointer. This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the data pointer by the Load-data-pointer command (see [Table 16 on page 12](#)).

Following this command, an arriving data byte is stored starting at the display RAM address indicated by the data pointer.

After each byte stored, the data pointer is automatically incremented in accordance with the chosen LCD multiplex drive mode configuration:

- by eight (static drive mode)
- by four (1:2 multiplex drive mode)
- by two (1:4 multiplex drive mode)
- by one or two (1:6 multiplex drive mode), see [Figure 37 on page 48](#)
- by one (1:8 multiplex drive mode)

When the address counter reaches the end of the RAM row, it stops incrementing after the last byte is transmitted. Redundant bits of the last byte transmitted are discarded. Additional bytes, sent after the end of the RAM is reached, will be discarded too. The data pointer does not wrap around to the beginning. To send new RAM data, the data pointer must be reset.

If an I²C-bus or SPI-bus data access is terminated early, then the state of the data pointer is unknown. The data pointer must then be re-written before further RAM accesses.

8.8.2 RAM filling in static drive mode

In the static drive mode the eight transmitted data bits are placed in eight successive display RAM columns in row 0 (see [Figure 33](#)).

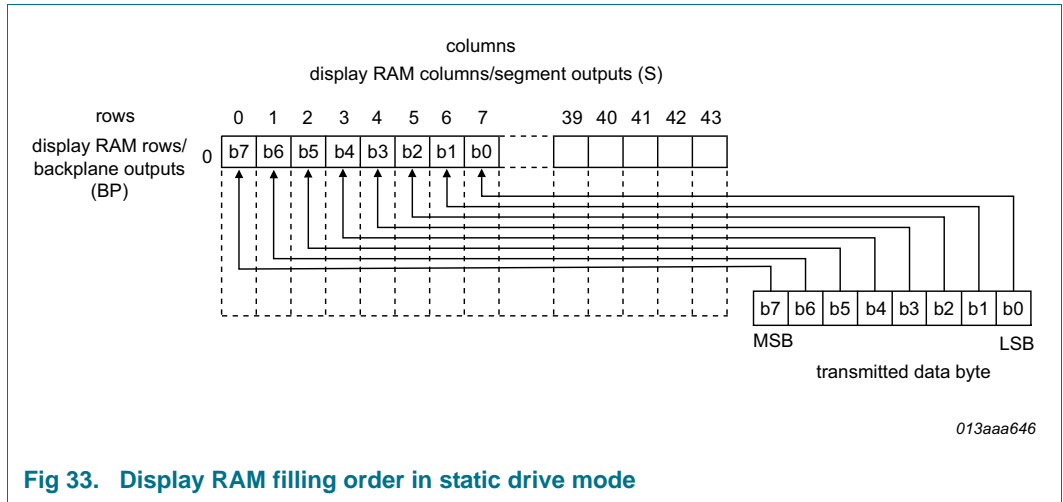


Fig 33. Display RAM filling order in static drive mode

In order to fill the whole RAM row, 6 bytes must be sent to the PCA8537, but the last 4 bits from the last byte are discarded (see Figure 34).

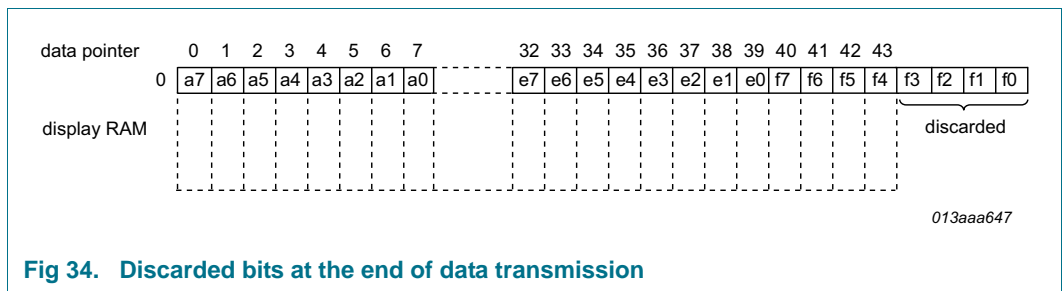


Fig 34. Discarded bits at the end of data transmission

When bit IBS is set to bank 1 (see Table 19 on page 14), then data is stored in row 4.

8.8.3 RAM filling in 1:2 multiplex drive mode

In the 1:2 multiplex drive mode the eight transmitted data bits are placed in four successive display RAM columns (see Figure 35). In order to fill the whole two RAM rows 11 bytes need to be sent to the PCA8537.

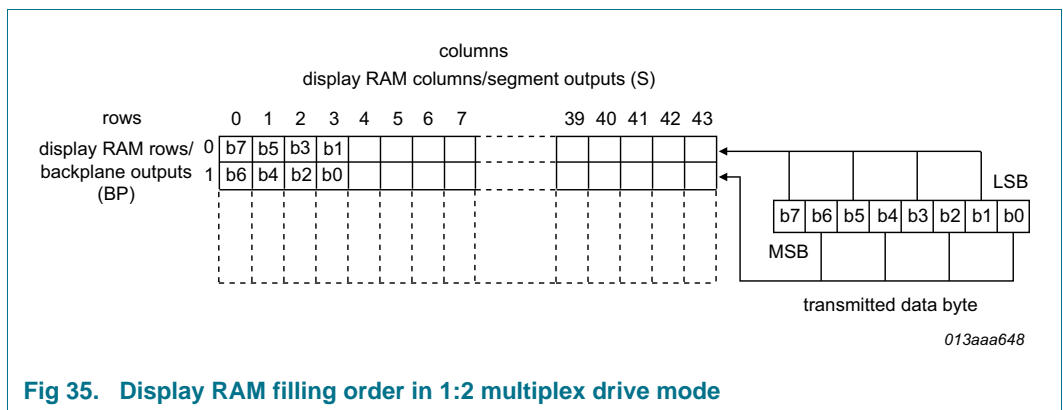
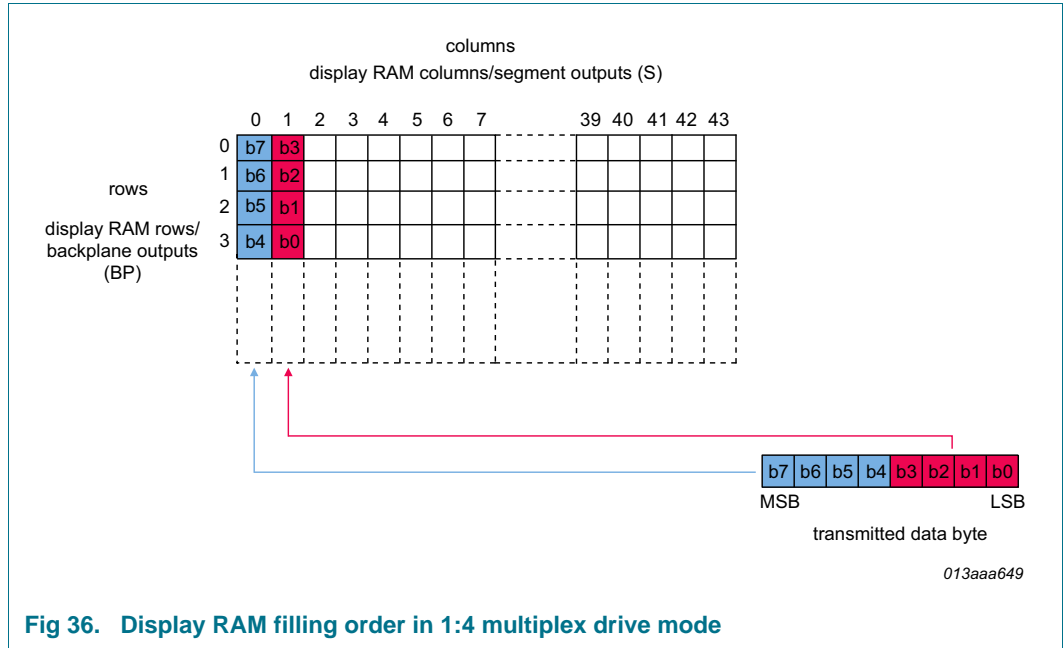


Fig 35. Display RAM filling order in 1:2 multiplex drive mode

When bit IBS is set to bank 1 (see Table 19 on page 14), then data is stored in row 4 and row 5.

8.8.4 RAM filling in 1:4 multiplex drive mode

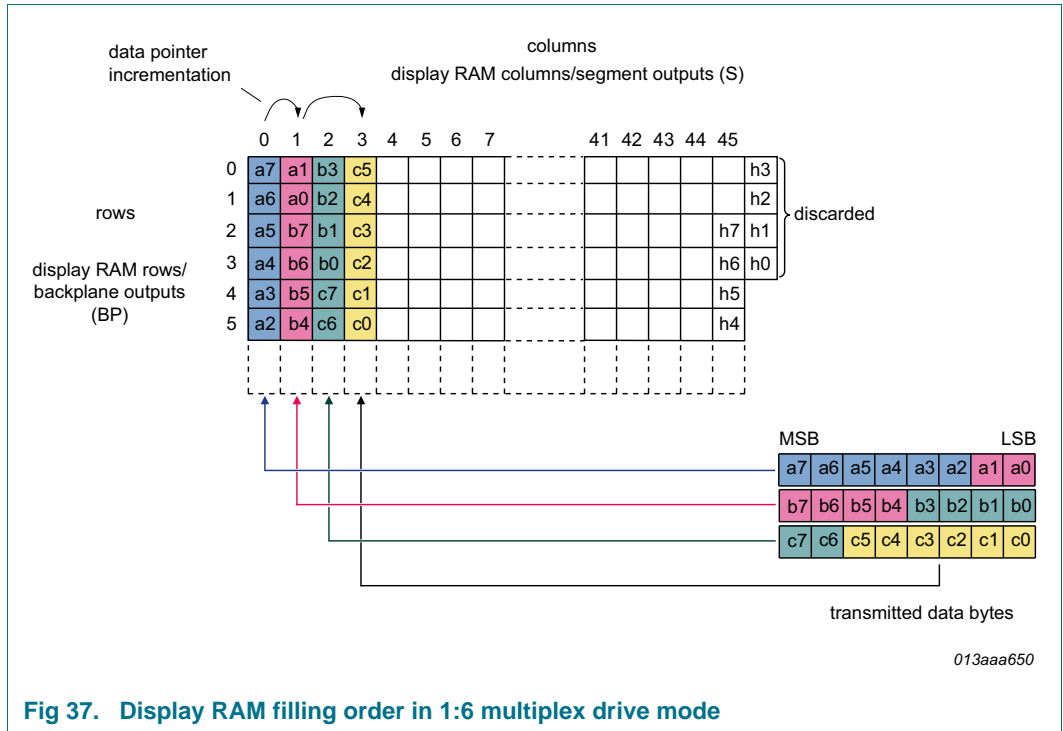
In the 1:4 multiplex drive mode the eight transmitted data bits are placed in two successive display RAM columns of four rows (see [Figure 36](#)). In order to fill the whole four RAM rows 22 bytes need to be sent to the PCA8537.



When bit IBS is set to bank 1 (see [Table 19 on page 14](#)), then data is stored in rows 4 to row 7.

8.8.5 RAM filling in 1:6 multiplex drive mode

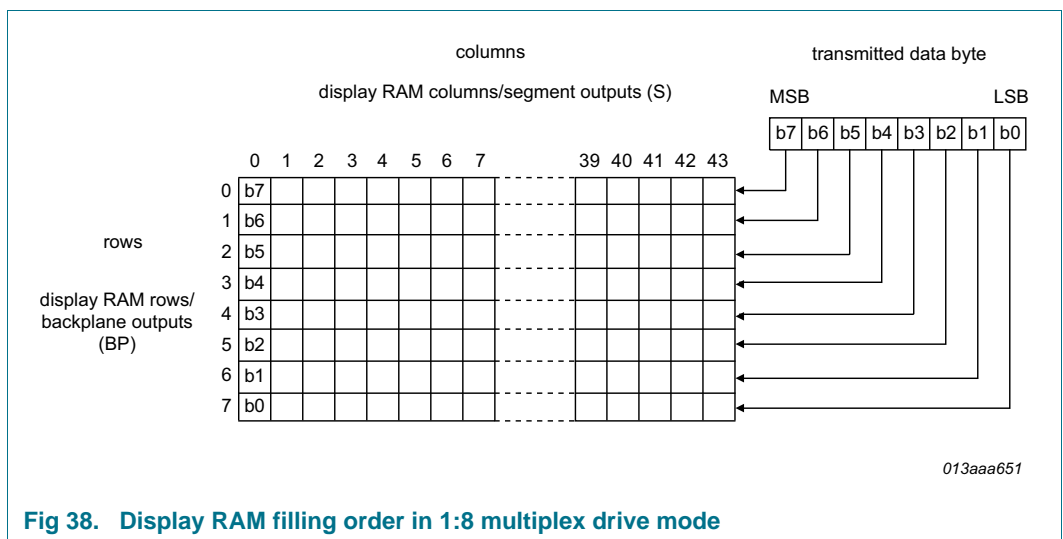
In the 1:6 multiplex drive mode the RAM is organized in six rows and 46 columns. The eight transmitted data bits are placed in such a way, that a column is filled up (see [Figure 37](#)). The remaining bits are wrapped up into the next column. In order to fill the whole RAM addresses 35 bytes need to be sent to the PCA8537, however the four least significant bits of the 35th byte are discarded.



When data transfer is initiated, then the MSB of the first byte will always be placed in row 0. Data must be transferred contiguously to achieve RAM filling as described in [Figure 37](#).

8.8.6 RAM filling in 1:8 multiplex drive mode

In the 1:8 multiplex drive mode the eight transmitted data bits are placed into eight rows of one display RAM column (see [Figure 38](#)). In order to fill the whole RAM addresses 44 bytes need to be sent to the PCA8537.



8.9 Bank selection

The PCA8537 includes a RAM bank switching feature in the static, 1:2, and 1:4 multiplex drive modes. A bank can be thought of as a collection of RAM rows. The RAM bank switching gives the provision for preparing display information in an alternative bank and to be able to switch to it once it is complete.

There are two banks; bank 0 and bank 1. [Figure 32 on page 44](#) shows the location of these banks relative to the RAM map. Input and output banks can be set independently from one another with the Bank-select command (see [Table 19 on page 14](#)). [Figure 39](#) shows the concept.

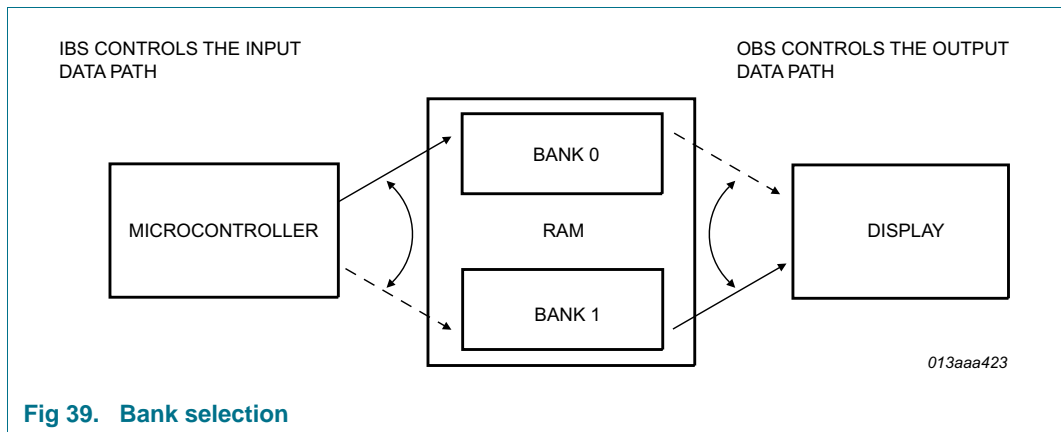


Fig 39. Bank selection

In [Figure 40](#) an example is shown for 1:4 multiplex drive mode where the displayed data is read from the first four rows of the memory (bank 0), while the transmitted data is stored in the second four rows of the memory (bank 1).

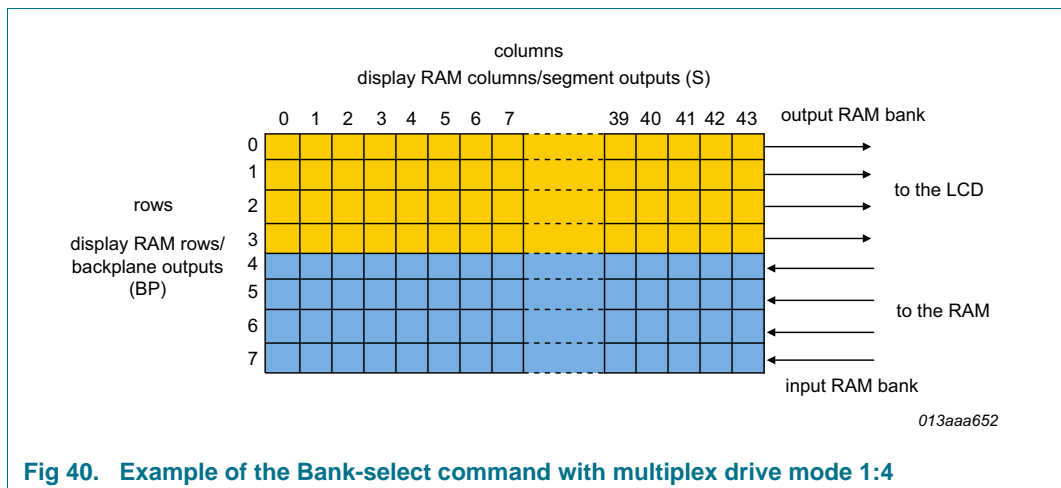


Fig 40. Example of the Bank-select command with multiplex drive mode 1:4

8.9.1 Input bank selection

The IBS (input bank selection) bit of the Bank-select command (see [Table 19](#)) controls where display data is loaded into the display RAM.

The input bank selection works independently of output bank selection.

8.9.2 Output bank selection

The OBS bit of the Bank-select command (see [Table 19 on page 14](#)) controls from which bank display data is taken,

The output bank selection works independently of input bank selection.

9. Bus interfaces

9.1 Control byte

After initiating the communication over the bus and sending the slave address (I²C-bus, see [Section 9.2](#)) or subaddress (SPI-bus, see [Section 9.3](#)), a control byte follows. The purpose of this byte is to indicate both, the content for the following data bytes (RAM or command) and to indicate that more control bytes will follow.

Typical sequences could be:

- Slave address/subaddress - control byte - command byte - command byte - command byte - end
- Slave address/subaddress - control byte - RAM byte - RAM byte - RAM byte - end
- Slave address/subaddress - control byte - command byte - control byte - RAM byte - end

In this way, it is possible to send a mixture of RAM and command data in one access or alternatively, to send just one type of data in one access.

Table 31. Control byte description

| Bit | Symbol | Binary value | Description |
|--------|--------|--------------|---------------------------|
| 7 | CO | | continue bit |
| | | 0 | last control byte |
| | | 1 | control bytes continue |
| 6 | RS | | register selection |
| | | 0 | command register |
| | | 1 | data register |
| 5 to 0 | - | | not relevant |

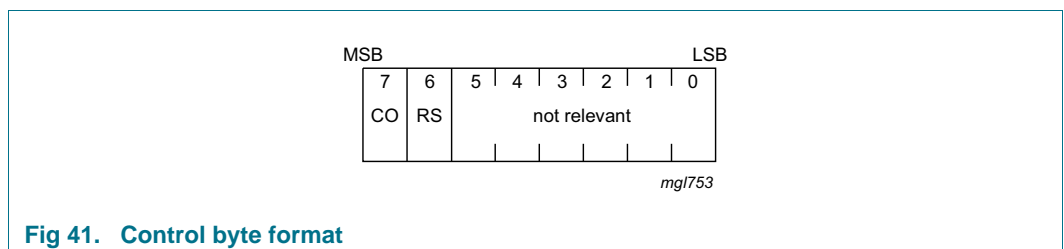


Fig 41. Control byte format

9.2 I²C-bus interface characteristics (PCA8537AH)

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a Serial Data line (SDA) and a Serial Clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

9.2.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal (see [Figure 42](#)).

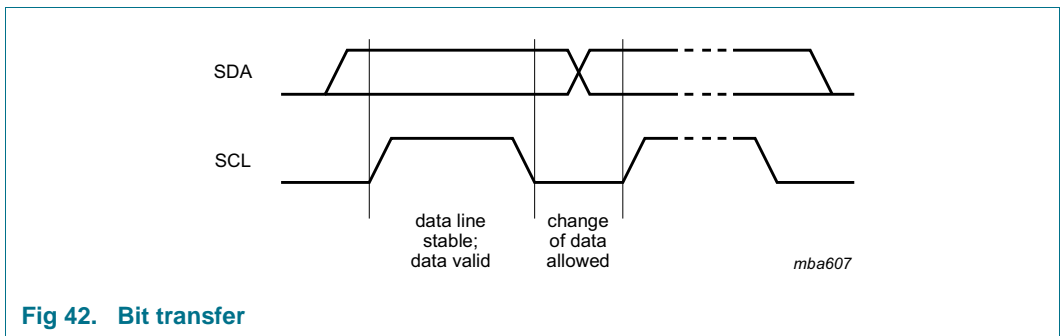


Fig 42. Bit transfer

9.2.2 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy.

A HIGH-to-LOW change of the data line, while the clock is HIGH is defined as the START condition (S).

A LOW-to-HIGH change of the data line while the clock is HIGH is defined as the STOP condition (P).

The START and STOP conditions are shown in [Figure 43](#).

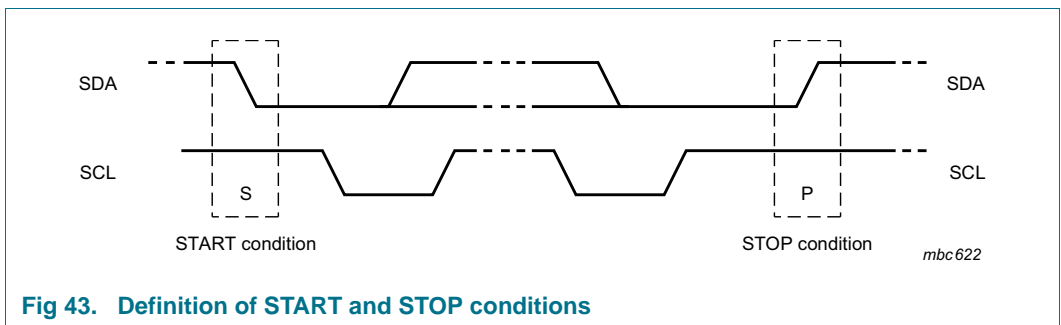


Fig 43. Definition of START and STOP conditions

9.2.3 System configuration

A device generating a message is a transmitter, a device receiving a message is the receiver. The device that controls the message is the master and the devices which are controlled by the master are the slaves. The system configuration is shown in [Figure 44](#).

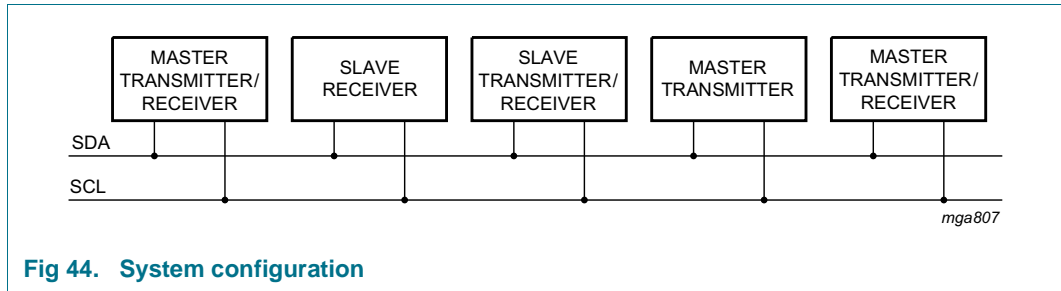


Fig 44. System configuration

9.2.4 Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of 8 bits is followed by an acknowledge cycle.

- A slave receiver which is addressed must generate an acknowledge after the reception of each byte.
- Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.
- The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be considered).
- A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

Acknowledgement on the I²C-bus is shown in [Figure 45](#).

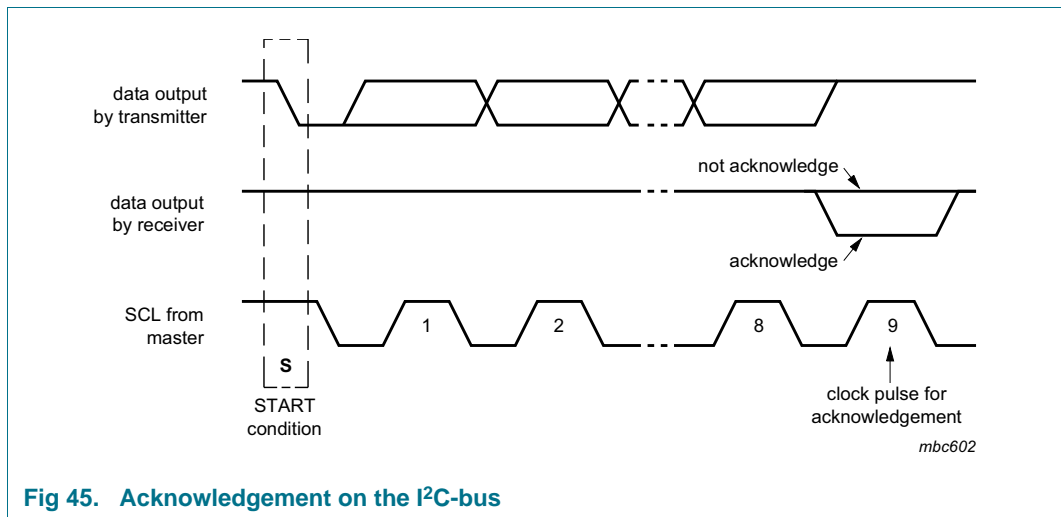


Fig 45. Acknowledgement on the I²C-bus

9.2.5 I²C-bus controller

The PCA8537AH acts as an I²C-bus slave receiver. It does not initiate I²C-bus transfers or transmit data to an I²C-bus master receiver. The only data output from PCA8537AH are the acknowledge signals and the temperature readout byte of the selected device.

9.2.6 Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

9.2.7 I²C-bus slave address

The device selection depends on the I²C-bus slave address.

Two different I²C-bus slave addresses can be used to address the PCA8537AH (see [Table 32](#)).

Table 32. I²C slave address byte

| Bit | Slave address | | | | | | | |
|-----|---------------|---|---|---|---|---|----|-----|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | MSB | | | | | | | LSB |
| | 0 | 1 | 1 | 1 | 0 | 0 | A0 | R/W |

Bit 1 of the slave address is defined by connecting the input A0 to either V_{SS} (logic 0) or V_{DD} (logic 1). Therefore, two instances of PCA8537AH can be distinguished on the same I²C-bus.

The least significant bit of the slave address byte is bit R/W (see [Table 33](#)).

Table 33. R/W bit description

| Symbol | Value | Description |
|--------|-------|-------------------------------------|
| R/W | | data read or write selection |
| | 0 | write data |
| | 1 | read data ^[1] |

[1] Only used for temperature readout from PCA8537AH (see [Table 21 on page 15](#)).

9.2.8 I²C-bus protocol

The I²C-bus protocol is shown in [Figure 46](#). The sequence is initiated with a START condition (S) from the I²C-bus master which is followed by one of the two PCA8537AH slave addresses available. All PCA8537AH's with the corresponding A0 level acknowledge in parallel to the slave address, but all PCA8537AH with an alternative A0 level ignore the whole I²C-bus transfer.

After acknowledgement, a control byte follows (see [Section 9.1 on page 50](#)).

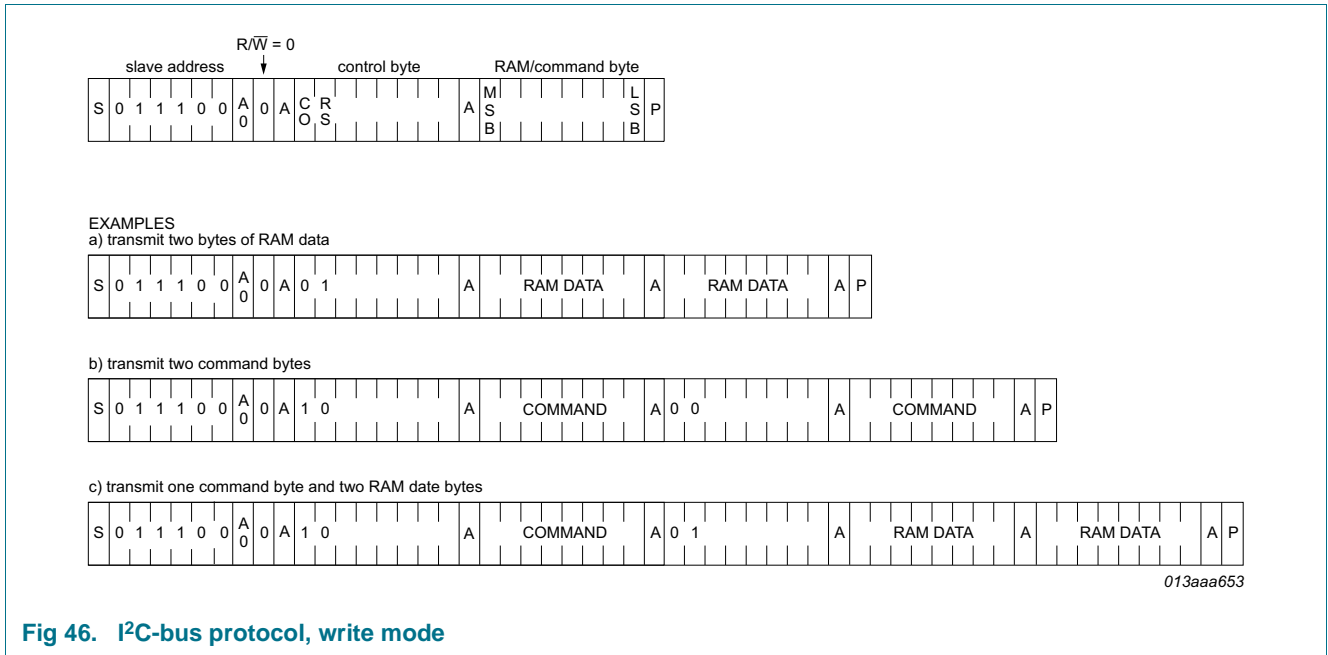


Fig 46. I²C-bus protocol, write mode

The display bytes are stored in the display RAM at the address specified by the data pointer.

The acknowledgement after each byte is made only by the addressed PCA8537AH. After the last display byte, the I²C-bus master issues a STOP condition (P). Alternatively a START may be issued to RESTART an I²C-bus access.

9.2.9 Data read

If a temperature readout (byte TD[7:0]) is made, the R/W bit must be logic 1 and then the next data byte following is provided by the PCA8537AH as shown in [Figure 47](#).

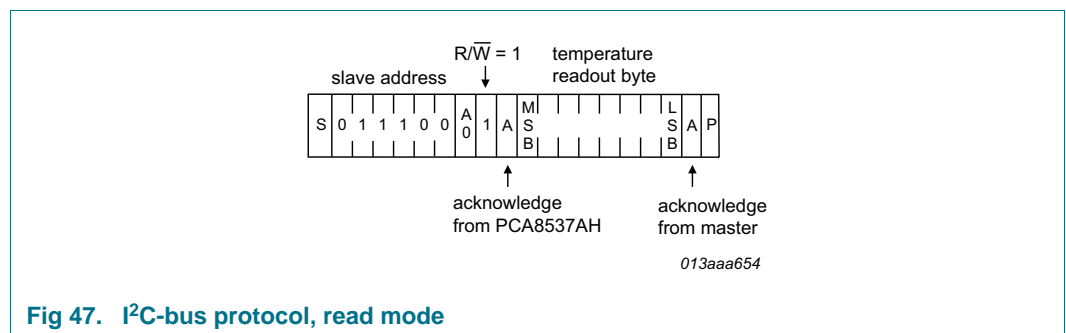


Fig 47. I²C-bus protocol, read mode

9.3 SPI-bus interface (PCA8537BH)

Data transfer to the device is made via a three-line SPI-bus (see [Table 31](#)). The SPI-bus is reset whenever the chip enable pin \overline{CE} is inactive.

Table 34. Serial interface

| Pin | Function | Description |
|-----------------|--|--|
| \overline{CE} | chip enable input; active LOW ^[1] | when HIGH, the interface is reset; |
| SCL | serial clock input | - |
| SDIO | serial data input output | input data is sampled on the rising edge of SCL; data is output on the falling edge of SCL |

[1] The chip enable must not be wired permanently LOW.

9.3.1 Data transmission

The chip enable signal is used to identify the transmitted data. Each data transfer is a byte, with the Most Significant Bit (MSB) sent first.

The transmission is controlled by the active LOW chip enable signal \overline{CE} . The first byte transmitted is the subaddress byte.

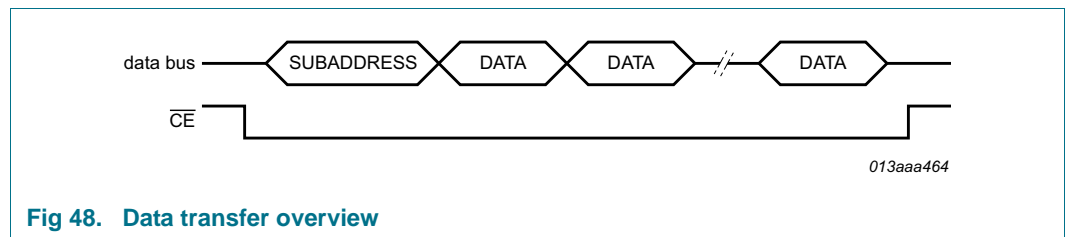


Fig 48. Data transfer overview

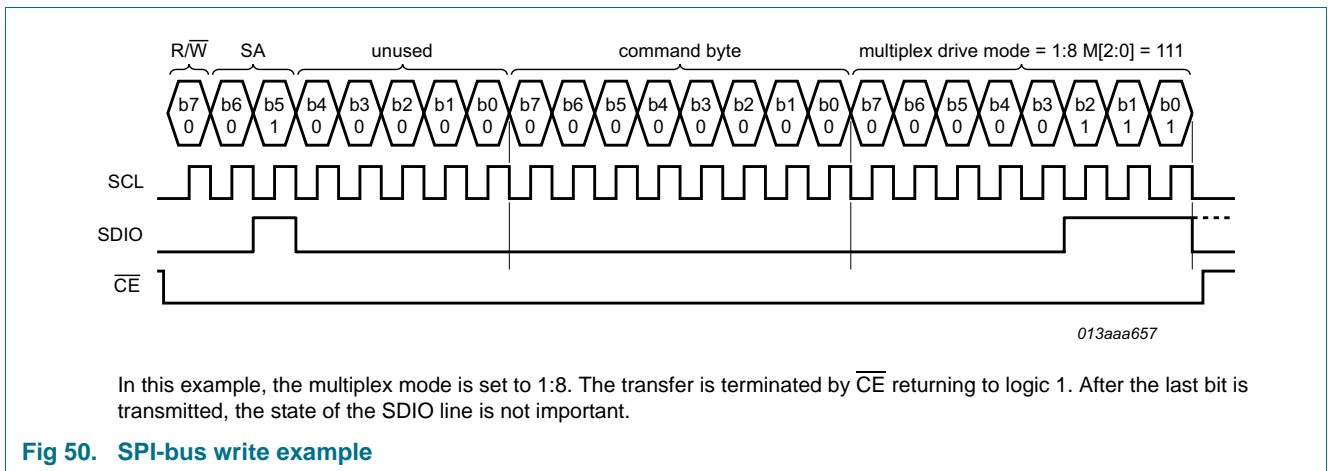
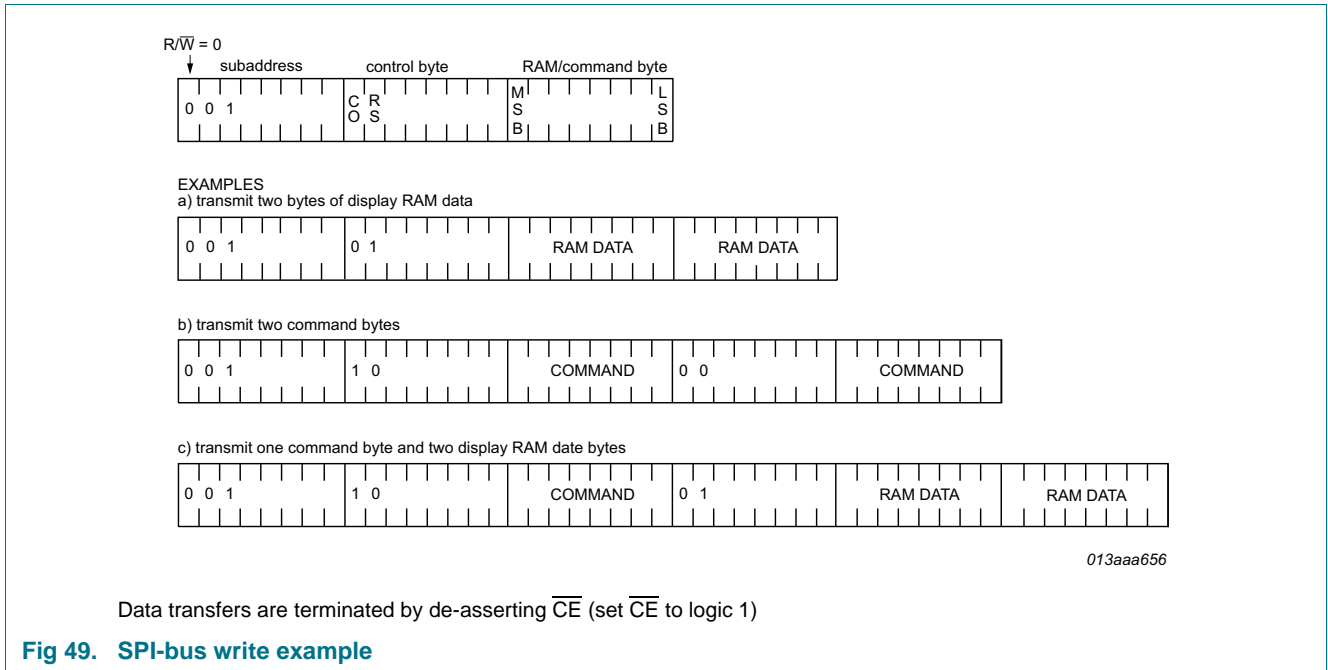
The subaddress byte opens the communication with a read/write bit and a subaddress. The subaddress is used to identify multiple devices on one SPI-bus.

Table 35. Subaddress byte definition

| Bit | Symbol | Binary value | Description |
|--------|---------|--------------|---|
| 7 | R/W | | data read or write selection |
| | | 0 | write data |
| | | 1 | read data ^[1] |
| 6 to 5 | SA[1:0] | 01 | subaddress ; other codes will cause the device to ignore data transfer |
| 4 to 0 | - | - | unused |

[1] Only used for temperature readout from PCA8537BH (see [Table 21 on page 15](#)).

After the subaddress byte, a control byte follows (see [Section 9.1 on page 50](#)).



9.3.2 Data read

The temperature readout data byte TD[7:0] can be read from the PCA8537BH.

A readout is initiated by sending the subaddress byte with the $\overline{R/W}$ bit set high. The transmission is controlled by the active LOW chip enable signal \overline{CE} .

After the last bit of the subaddress byte is transmitted, the PCA8537BH will immediately start to drive the SDIO line. It is only necessary to read the values once, however since the update of the register is asynchronous to the interface clock, it is recommended to read the register twice and check for a stable value.

The readout is terminated by asserting \overline{CE} . At this time, the SDIO bus is released. It is important that the bus is not left floating and that the microcontroller then takes over driving of the bus.

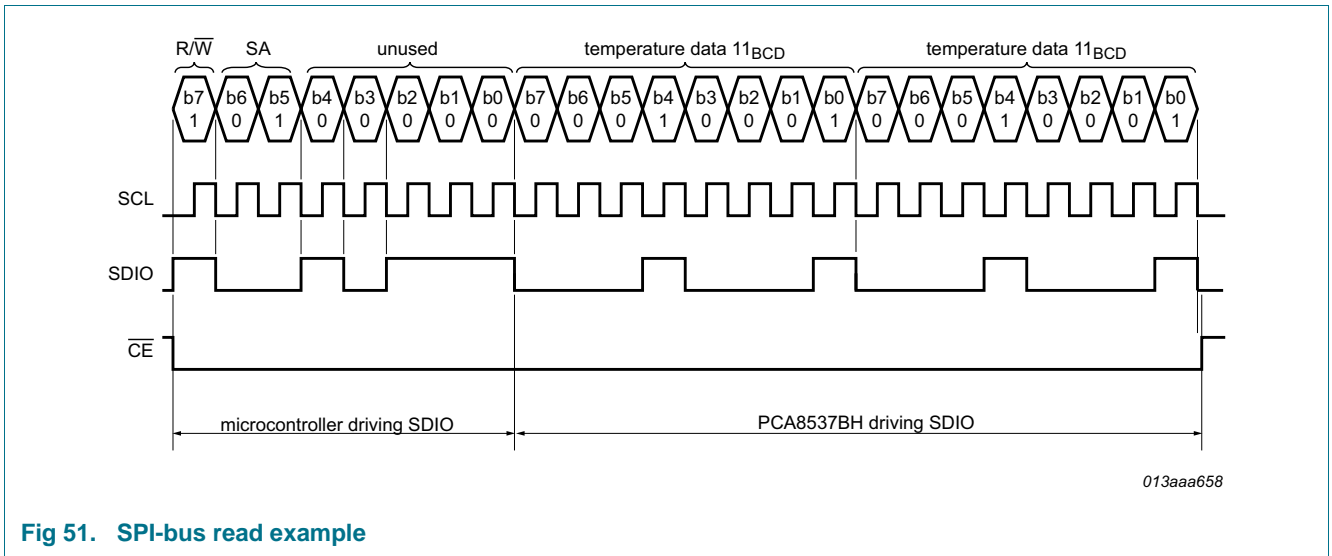
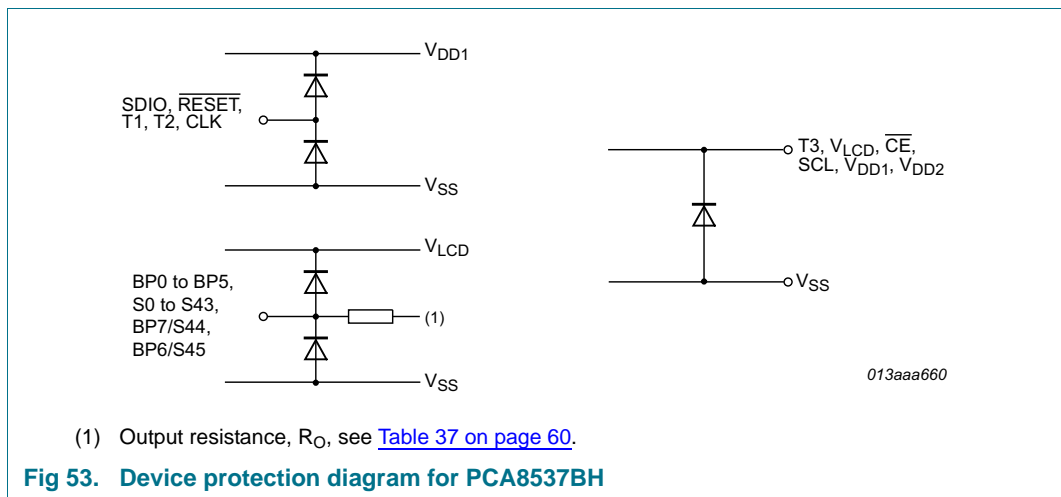
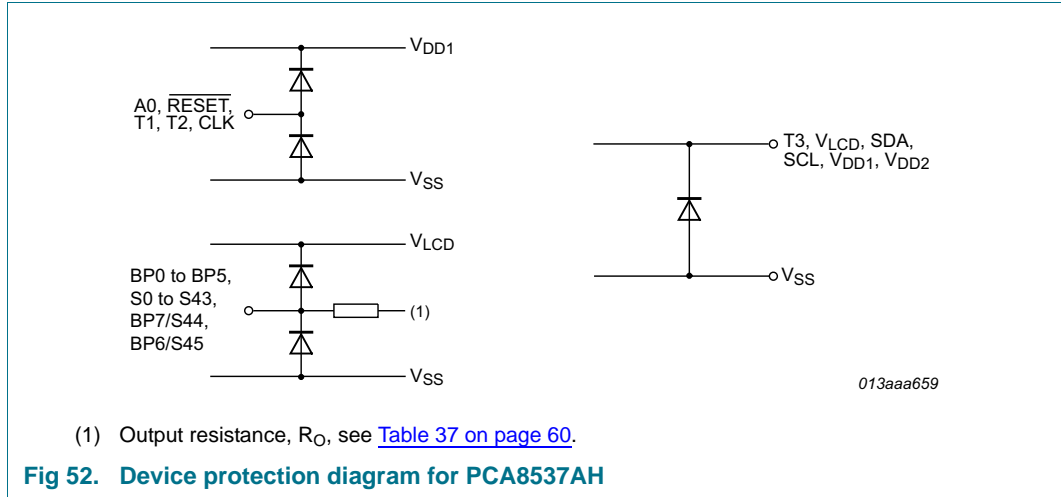


Fig 51. SPI-bus read example

10. Internal circuitry



11. Safety notes

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices. Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

CAUTION



Static voltages across the liquid crystal display can build up when the LCD supply voltage (V_{LCD}) is on while the IC supply voltage (V_{DD}) is off, or vice versa. This may cause unwanted display artifacts. To avoid such artifacts, V_{LCD} and V_{DD} must be applied or removed together.

12. Limiting values

Table 36. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|----------------------|---------------------------------|--|------|-------|------|
| V _{DD1} | supply voltage 1 | digital | -0.5 | +6.5 | V |
| V _{DD2} | supply voltage 2 | analog | -0.5 | +6.5 | V |
| I _{DD1} | supply current 1 | digital | -50 | +50 | mA |
| I _{DD2} | supply current 2 | analog | -50 | +50 | mA |
| V _{LCD} | LCD supply voltage | | -0.5 | +10 | V |
| I _{DD(LCD)} | LCD supply current | | -50 | +50 | mA |
| V _i | input voltage | on pins CLK, $\overline{\text{CE}}$, SDA, SCL, A0, SDIO, T1, T2 | -0.5 | +6.5 | V |
| I _i | input current | | -10 | +10 | mA |
| V _O | output voltage | on pins S0 to S45, BP0 to BP7 | -0.5 | +10 | V |
| | | on pins SDA, SDIO, CLK | -0.5 | +6.5 | V |
| I _O | output current | | -10 | +10 | mA |
| I _{SS} | ground supply current | | -50 | +50 | mA |
| P _{tot} | total power dissipation | | - | 400 | mW |
| P/out | power dissipation per output | | - | 100 | mW |
| V _{ESD} | electrostatic discharge voltage | HBM [1] | - | ±4500 | V |
| | | CDM [2] | - | ±1500 | V |
| I _{lu} | latch-up current | [3] | - | 200 | mA |
| T _{stg} | storage temperature | [4] | -65 | +150 | °C |
| T _{amb} | ambient temperature | operating device | -40 | +95 | °C |

[1] Pass level; Human Body Model (HBM), according to [Ref. 6 "JESD22-A114"](#).

[2] Pass level; Charged-Device Model (CDM), according to [Ref. 7 "JESD22-C101"](#).

[3] Pass level; latch-up testing according to [Ref. 8 "JESD78"](#) at maximum ambient temperature (T_{amb(max)}).

[4] According to the NXP store and transport requirements (see [Ref. 10 "NX3-00092"](#)) the devices have to be stored at a temperature of +8 °C to +45 °C and a humidity of 25 % to 75 %. For long term storage products deviant conditions are described in that document.

13. Static characteristics

Table 37. Static characteristics

$V_{DD1} = 1.8\text{ V to }5.5\text{ V}$; $V_{DD2} = 2.5\text{ V to }5.5\text{ V}$; $V_{SS} = 0\text{ V}$; $V_{LCD} = 2.5\text{ V to }9.0\text{ V}$; $T_{amb} = -40\text{ °C to }+95\text{ °C}$; temperature measurement enabled; 1:8 multiplex drive mode; $\frac{1}{4}$ bias; LCD outputs are open circuit; RAM is all written with logic 1; inputs at V_{SS} or V_{DD} ; internal clock with maximum prescale factor; I²C-bus/SPI-bus inactive; unless otherwise specified.

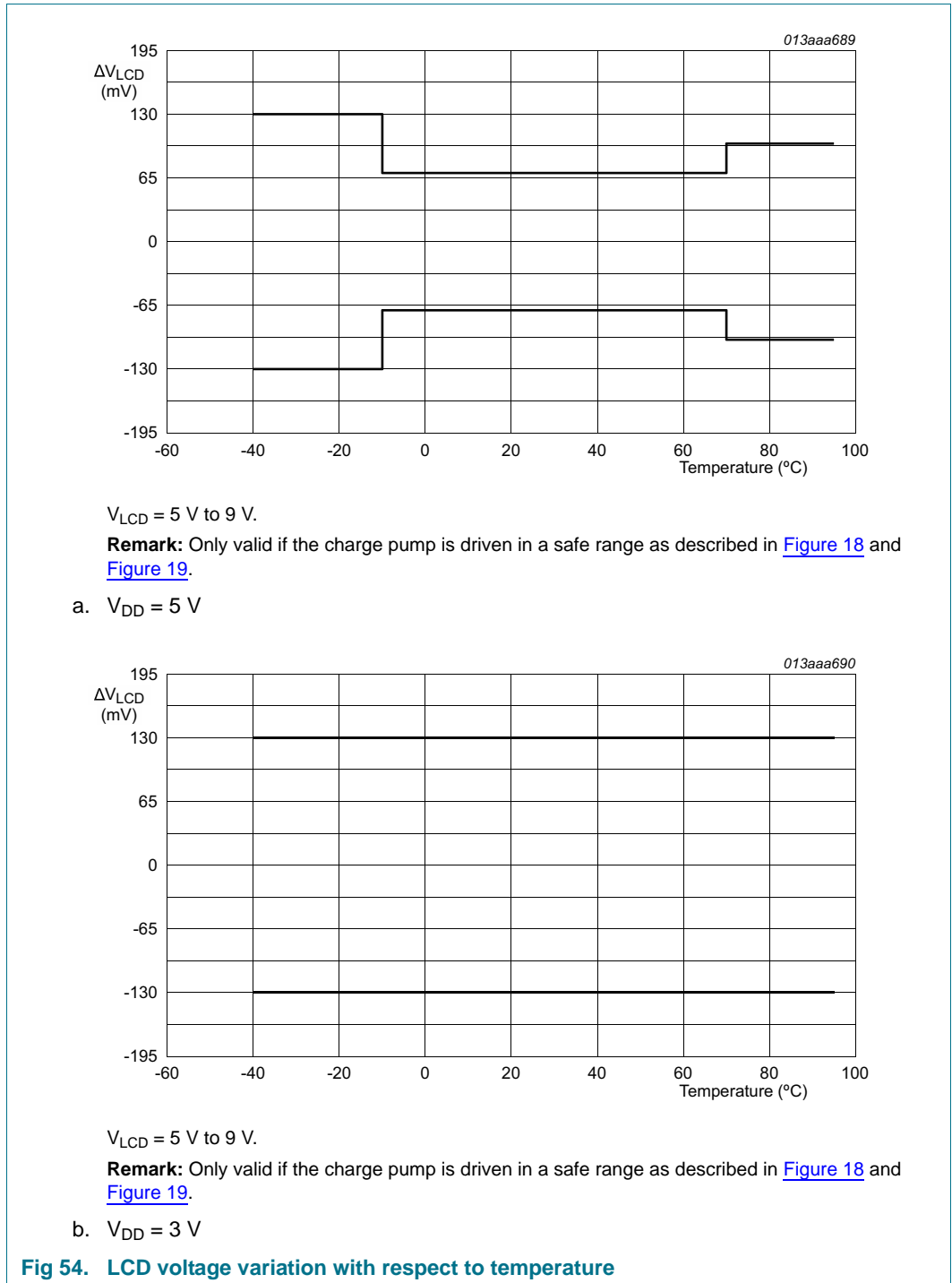
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------|--------------------------------|--|----------------|-----|----------------|--------------------|
| Supplies | | | | | | |
| V_{DD1} | supply voltage 1 | logic | 1.8 | - | 5.5 | V |
| V_{DD2} | supply voltage 2 | analog; $V_{DD2} \geq V_{DD1}$ | | | | |
| | | charge pump set to $2 \times V_{DD2}$ | 2.5 | - | 5.5 | V |
| | | charge pump set to $3 \times V_{DD2}$ | 2.5 | - | 5.5 | V |
| V_{LCD} | LCD supply voltage | $V_{LCD} \geq V_{DD2}$ | [1] 2.5 | - | 9.0 | V |
| ΔV_{LCD} | LCD voltage variation | $V_{DD1} = V_{DD2} = 5.0\text{ V}$; $V_{LCD} = 6.99\text{ V}$ | [2] -0.10 | - | +0.10 | V |
| I_{DD1} | supply current 1 | digital; display disabled; charge pump off | - | 90 | 200 | μA |
| I_{DD2} | supply current 2 | display disabled; charge pump off; external V_{LCD} | - | 0.5 | - | μA |
| | | $V_{DD2} = 5.5\text{ V}$; charge pump set to $2 \times V_{DD2}$; internal $V_{LCD} = 7.0\text{ V}$ | | | | |
| | | display disabled | - | 30 | 40 | μA |
| | | display enabled | [3] - | 200 | - | μA |
| $I_{DD(LCD)}$ | LCD supply current | external $V_{LCD} = 7.0\text{ V}$; display enabled; | - | 85 | - | μA |
| $I_{DD(pd)}$ | power-down mode supply current | on pin V_{DD1} | - | 1 | 3 | μA |
| $I_{LCD(pd)}$ | power-down LCD current | | - | 15 | 25 | μA |
| T_{acc} | temperature accuracy | readout temperature error; $V_{DD1} = 5.0\text{ V}$ | | | | |
| | | $T_{amb} = -40\text{ °C to }+95\text{ °C}$ | -5 | - | +5 | $^{\circ}\text{C}$ |
| | | $T_{amb} = 25\text{ °C}$ | -3 | - | +3 | $^{\circ}\text{C}$ |
| Logic | | | | | | |
| V_I | input voltage | | $V_{SS} - 0.5$ | - | $V_{DD} + 0.5$ | V |
| V_{IL} | LOW-level input voltage | on pins CLK and A0 | - | - | $0.3V_{DD}$ | V |
| V_{IH} | HIGH-level input voltage | on pins CLK and A0 | $0.7V_{DD}$ | - | - | V |
| V_O | output voltage | | -0.5 | - | $V_{DD} + 0.5$ | V |
| V_{OH} | HIGH-level output voltage | on pin CLK | $0.8V_{DD}$ | - | - | V |
| V_{OL} | LOW-level output voltage | on pin CLK | - | - | $0.2V_{DD}$ | V |
| I_{OH} | HIGH-level output current | output source current; $V_{OH} = 4.6\text{ V}$; $V_{DD} = 5\text{ V}$; on pin CLK | 1 | - | - | mA |

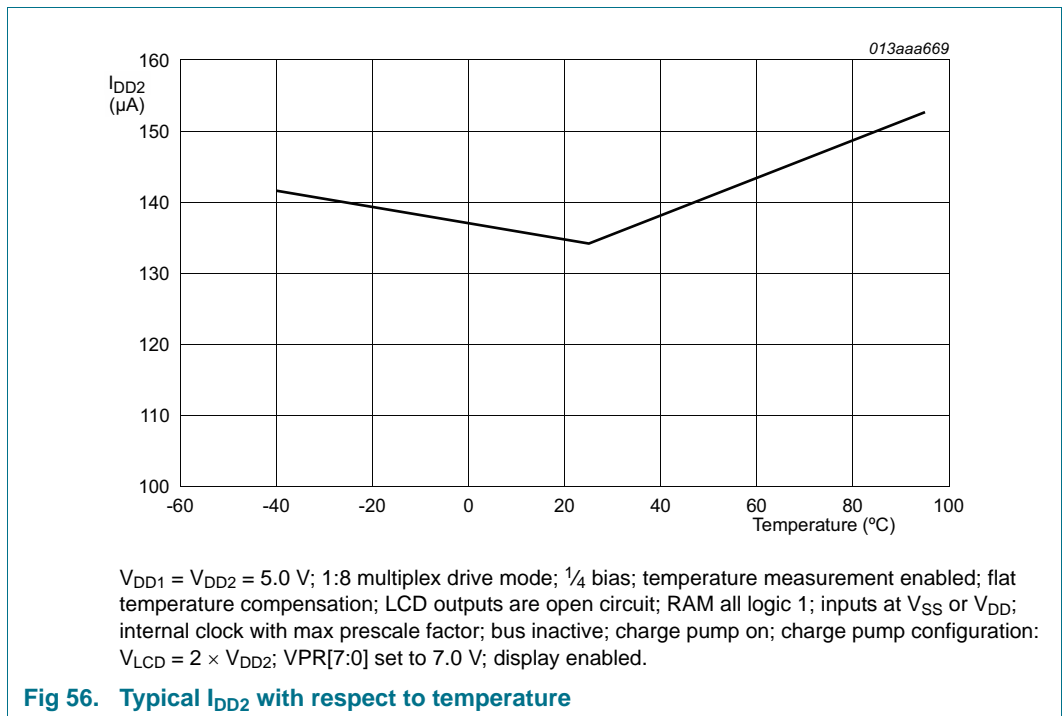
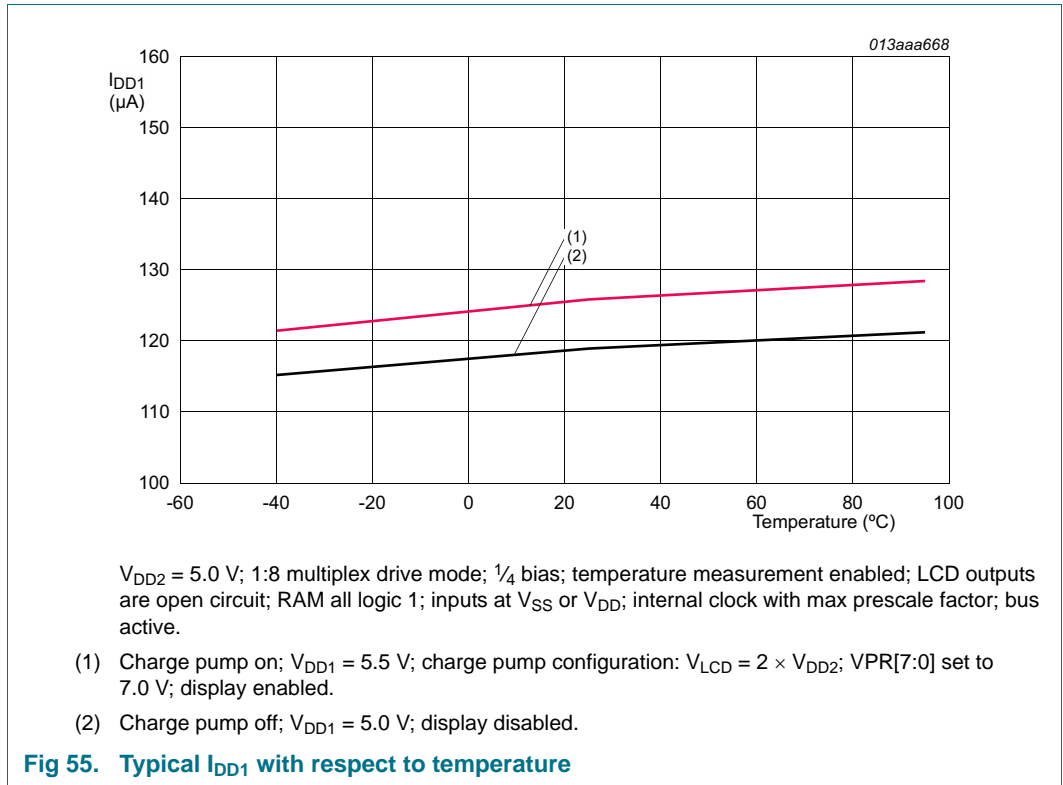
Table 37. Static characteristics ...continued

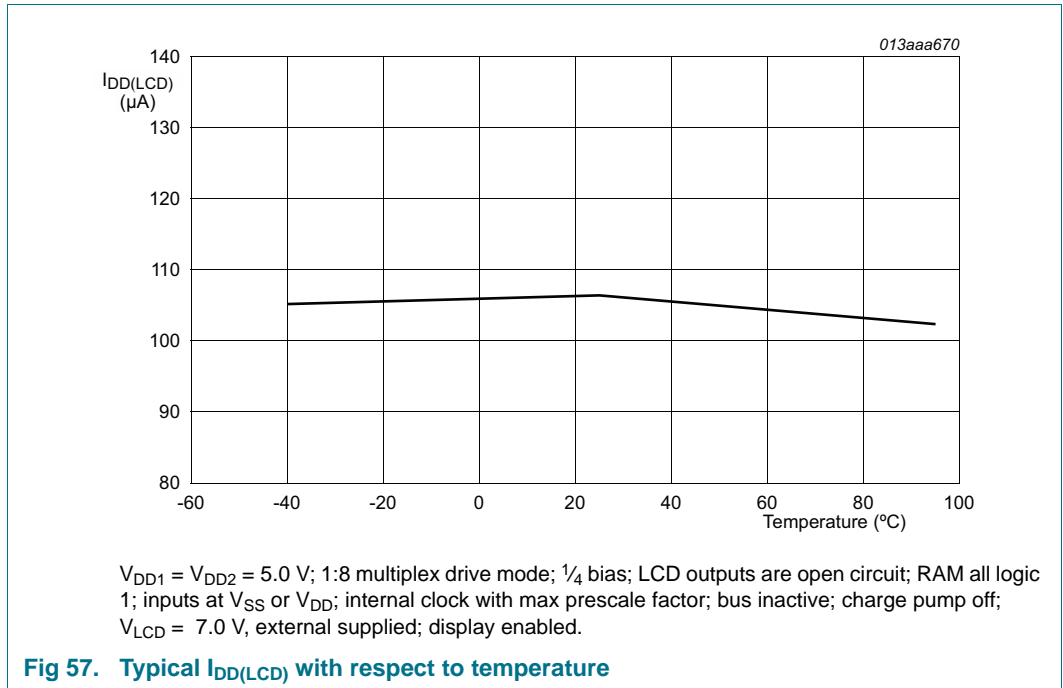
$V_{DD1} = 1.8\text{ V to }5.5\text{ V}$; $V_{DD2} = 2.5\text{ V to }5.5\text{ V}$; $V_{SS} = 0\text{ V}$; $V_{LCD} = 2.5\text{ V to }9.0\text{ V}$; $T_{amb} = -40\text{ }^{\circ}\text{C to }+95\text{ }^{\circ}\text{C}$; temperature measurement enabled; 1:8 multiplex drive mode; $1/4$ bias; LCD outputs are open circuit; RAM is all written with logic 1; inputs at V_{SS} or V_{DD} ; internal clock with maximum prescale factor; $I^2\text{C}$ -bus/SPI-bus inactive; unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit | |
|--|---------------------------|--|----------------|-----|----------------|---------------|------------------|
| I_{OL} | LOW-level output current | output sink current; $V_{OL} = 0.4\text{ V}$; $V_{DD} = 5\text{ V}$; on pin CLK | 1 | - | - | mA | |
| V_{POR} | power-on reset voltage | [4] | - | - | 1.6 | V | |
| I_L | leakage current | $V_i = V_{DD}$ or V_{SS} ; on pins CLK and A0 | -1 | - | +1 | μA | |
| I²C- and SPI-bus lines; pins SDA, SCL and SDIO | | | | | | | |
| V_i | input voltage | | | | | | |
| | | pins SDA, SCL | $V_{SS} - 0.5$ | - | 5.5 | V | |
| | | pin SDIO | $V_{SS} - 0.5$ | - | $V_{DD} + 0.5$ | V | |
| V_{IL} | LOW-level input voltage | pins SDA, SCL, and SDIO | - | - | $0.3V_{DD}$ | V | |
| V_{IH} | HIGH-level input voltage | pins SDA, SCL, and SDIO | $0.7V_{DD}$ | - | - | V | |
| V_O | output voltage | | | | | | |
| | | pins SDA and SCL | -0.5 | - | 5.5 | V | |
| | | SDIO | -0.5 | - | $V_{DD} + 0.5$ | V | |
| I_{OL} | LOW-level output current | $V_{OL} = 0.4\text{ V}$; $V_{DD} = 5\text{ V}$; on pin SDA and SDIO | 3 | - | - | mA | |
| I_{OH} | HIGH-level output current | $V_{OH} = 4.6\text{ V}$; $V_{DD} = 5\text{ V}$; on pin SDIO | 3 | - | - | mA | |
| I_L | leakage current | $V_i = V_{DD}$ or V_{SS} | -1 | - | +1 | μA | |
| LCD outputs | | | | | | | |
| ΔV_O | output voltage variation | on pins BP0 to BP7 | [5] | -15 | - | +15 | mV |
| | | on pins S0 to S45 | [6] | -15 | - | +15 | mV |
| R_O | output resistance | $V_{LCD} = 7\text{ V}$; on pins BP0 to BP7 | [7] | 0.3 | 0.8 | 1.5 | $\text{k}\Omega$ |
| | | $V_{LCD} = 7\text{ V}$; on pins S0 to S45 | [7] | 0.6 | 1.5 | 3 | $\text{k}\Omega$ |

- [1] When supplying external V_{LCD} it must be $V_{LCD} \geq V_{DD2}$. Also when using the internal charge pump to generate a certain V_{LCD} , $VPR[7:0]$ must be set to a value that the voltage is higher than V_{DD2} (see [Section 8.4.2](#)).
- [2] Calibrated at testing stage. V_{LCD} temperature compensation is disabled.
- [3] Tested on sample basis.
- [4] If $V_{DD1} < V_{POR}$ a reset occurs.
- [5] Variation between any 2 backplanes on a given voltage level; static measured.
- [6] Variation between any 2 segments on a given voltage level; static measured.
- [7] Outputs measured one at a time.







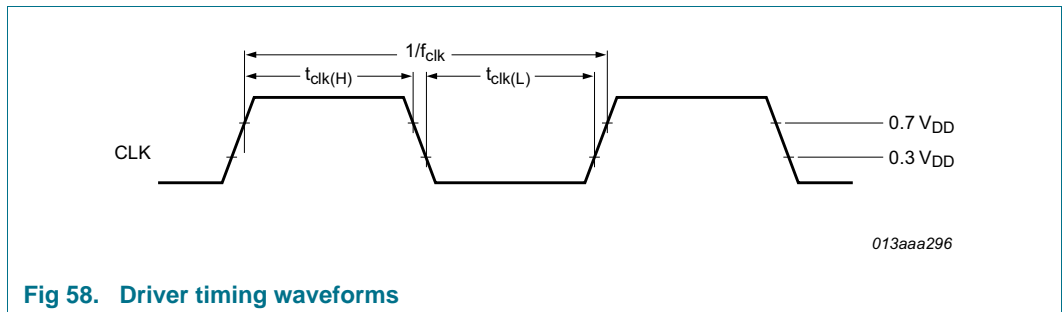
14. Dynamic characteristics

Table 38. Dynamic characteristics

$V_{DD} = 1.8 V$ to $5.5 V$; $V_{SS} = 0 V$; $V_{LCD} = 2.5 V$ to $9.0 V$; $T_{amb} = -40^{\circ}C$ to $+95^{\circ}C$; unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------|--------------------------|--|----------|------|-------|---------|
| $f_{clk(ext)}$ | external clock frequency | | 450 | - | 14500 | Hz |
| $t_{clk(H)}$ | clock HIGH time | external clock source used | 33 | - | - | μs |
| $t_{clk(L)}$ | clock LOW time | | 33 | - | - | μs |
| f_{clk} | clock frequency | on pin CLK; see Table 18 | [1] 7800 | 9600 | 11040 | Hz |
| $t_{w(rst)L}$ | LOW-level reset time | | 400 | - | - | ns |

[1] Frequency present on OSCCLK with default display frequency division factor.



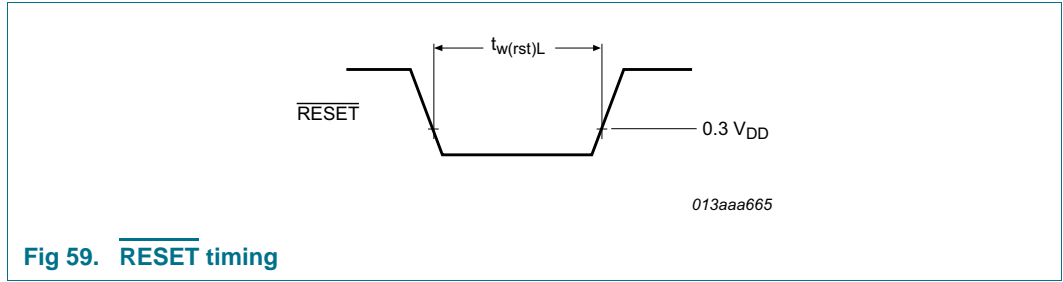


Table 39. Timing characteristics: I²C-bus

$V_{DD1} = 1.8\text{ V to }5.5\text{ V}$; $V_{DD2} = 2.5\text{ V to }5.5\text{ V}$; $V_{SS} = 0\text{ V}$; $T_{amb} = -40\text{ °C to }+95\text{ °C}$; unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------------|--|-----------------------------|-----|-----|-----|------|
| f _{SCL} | SCL clock frequency | | - | - | 400 | kHz |
| t _{BUF} | bus free time between a STOP and START condition | | 1.3 | - | - | μs |
| t _{HD;STA} | hold time (repeated) START condition | | 0.6 | - | - | μs |
| t _{SU;STA} | set-up time for a repeated START condition | | 0.6 | - | - | μs |
| t _{VD;DAT} | data valid time | [4] | - | - | 0.9 | μs |
| t _{VD;ACK} | data valid acknowledge time | [5] | - | - | 0.9 | μs |
| t _{LOW} | LOW period of the SCL clock | | 1.3 | - | - | μs |
| t _{HIGH} | HIGH period of the SCL clock | | 0.6 | - | - | μs |
| t _f | fall time | of both SDA and SCL signals | - | - | 0.3 | μs |
| t _r | rise time | of both SDA and SCL signals | - | - | 0.3 | μs |
| C _b | capacitive load for each bus line | | - | - | 400 | pF |
| t _{SU;DAT} | data set-up time | | 100 | - | - | ns |
| t _{HD;DAT} | data hold time | | 0 | - | - | ns |
| t _{SU;STO} | set-up time for STOP condition | | 0.6 | - | - | μs |
| t _{w(spike)} | spike pulse width | | - | - | 50 | ns |

- [1] Internal calibration made with OTP so that the maximum variation is ±15 % over whole temperature and voltage range. The typical f_{clk} frequency generates a typical frame frequency of 200 Hz when the default frequency division factor is used.
- [2] The typical value is defined at V_{DD1} = V_{DD2} = 5.0 V and 30 °C.
- [3] All timing values are valid within the operating supply voltage and ambient temperature range and are referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.
- [4] t_{VD;DAT} = minimum time for valid SDA output following SCL LOW.
- [5] t_{VD;ACK} = time for acknowledgement signal from SCL LOW to SDA output LOW.

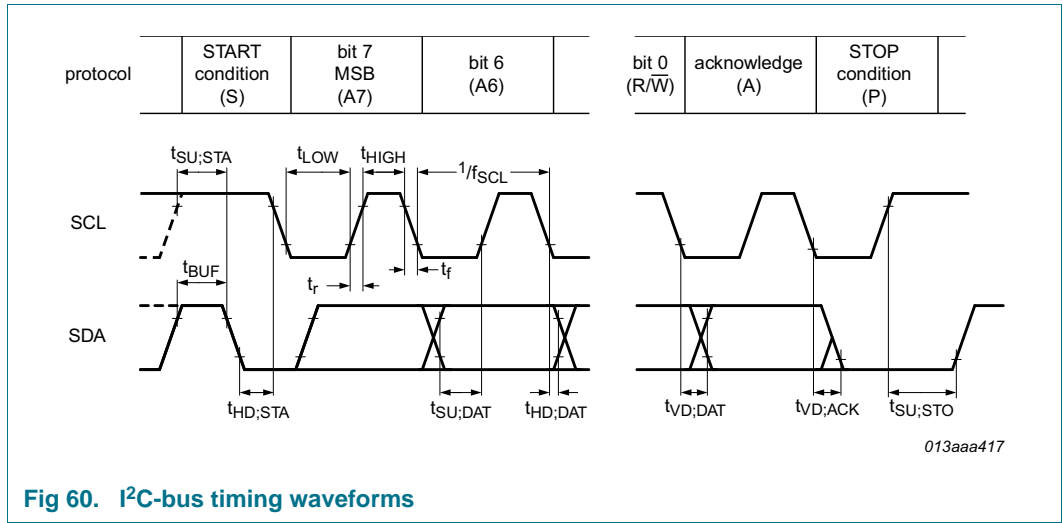


Fig 60. I²C-bus timing waveforms

Table 40. Timing characteristics: SPI-bus

$V_{DD} = 1.8\text{ V to }5.5\text{ V}$; $V_{SS} = 0\text{ V}$; $T_{amb} = -40\text{ }^{\circ}\text{C to }+95\text{ }^{\circ}\text{C}$. All timing values are valid within the operating supply voltage and temperature range and referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD} .

| Symbol | Parameter | Conditions | $V_{DD} < 2.7\text{ V}$ | | $V_{DD} \geq 2.7\text{ V}$ | | Unit |
|---|-------------------------------|--------------------------|-------------------------|-----|----------------------------|-----|------|
| | | | Min | Max | Min | Max | |
| Timing characteristics (see Figure 61) | | | | | | | |
| $f_{clk(SCL)}$ | SCL clock frequency | | - | 2 | - | 5 | MHz |
| t_{SCL} | SCL time | | 500 | - | 200 | - | ns |
| $t_{clk(H)}$ | clock HIGH time | | 200 | - | 80 | - | ns |
| $t_{clk(L)}$ | clock LOW time | | 200 | - | 80 | - | ns |
| t_r | rise time | for SCL signal | - | 100 | - | 100 | ns |
| t_f | fall time | for SCL signal | - | 100 | - | 100 | ns |
| $t_{su}(\overline{CE})$ | \overline{CE} set-up time | | 150 | - | 80 | - | ns |
| $t_h(\overline{CE})$ | \overline{CE} hold time | | 0 | - | 0 | - | ns |
| $t_{rec}(\overline{CE})$ | \overline{CE} recovery time | | 100 | - | 100 | - | ns |
| t_{su} | set-up time | set-up time for SDI data | 35 | - | 10 | - | ns |
| t_h | hold time | hold time for SDI data | 25 | - | 15 | - | ns |

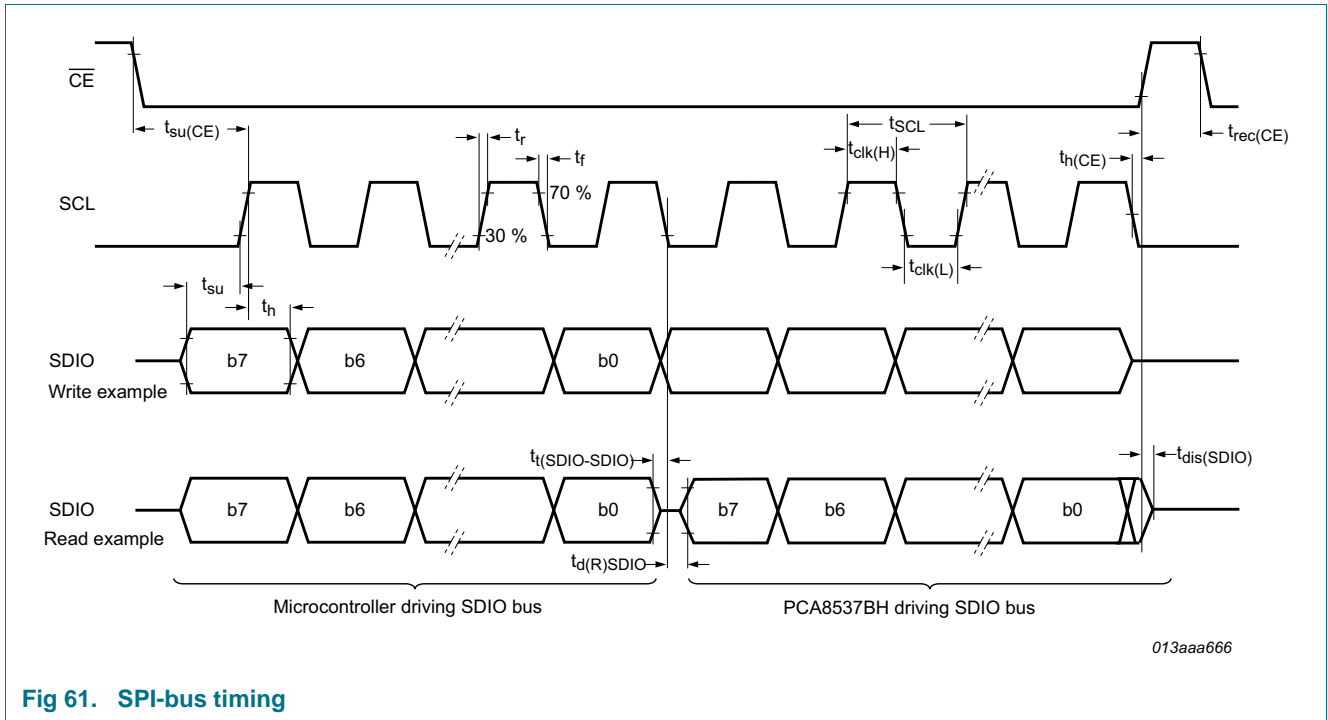


Fig 61. SPI-bus timing

15. Test information

15.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q100 - *Failure mechanism based stress test qualification for integrated circuits*, and is suitable for use in automotive applications.

16. Package outline

TQFP64: plastic thin quad flat package; 64 leads; body 10 x 10 x 1.0 mm

SOT357-1

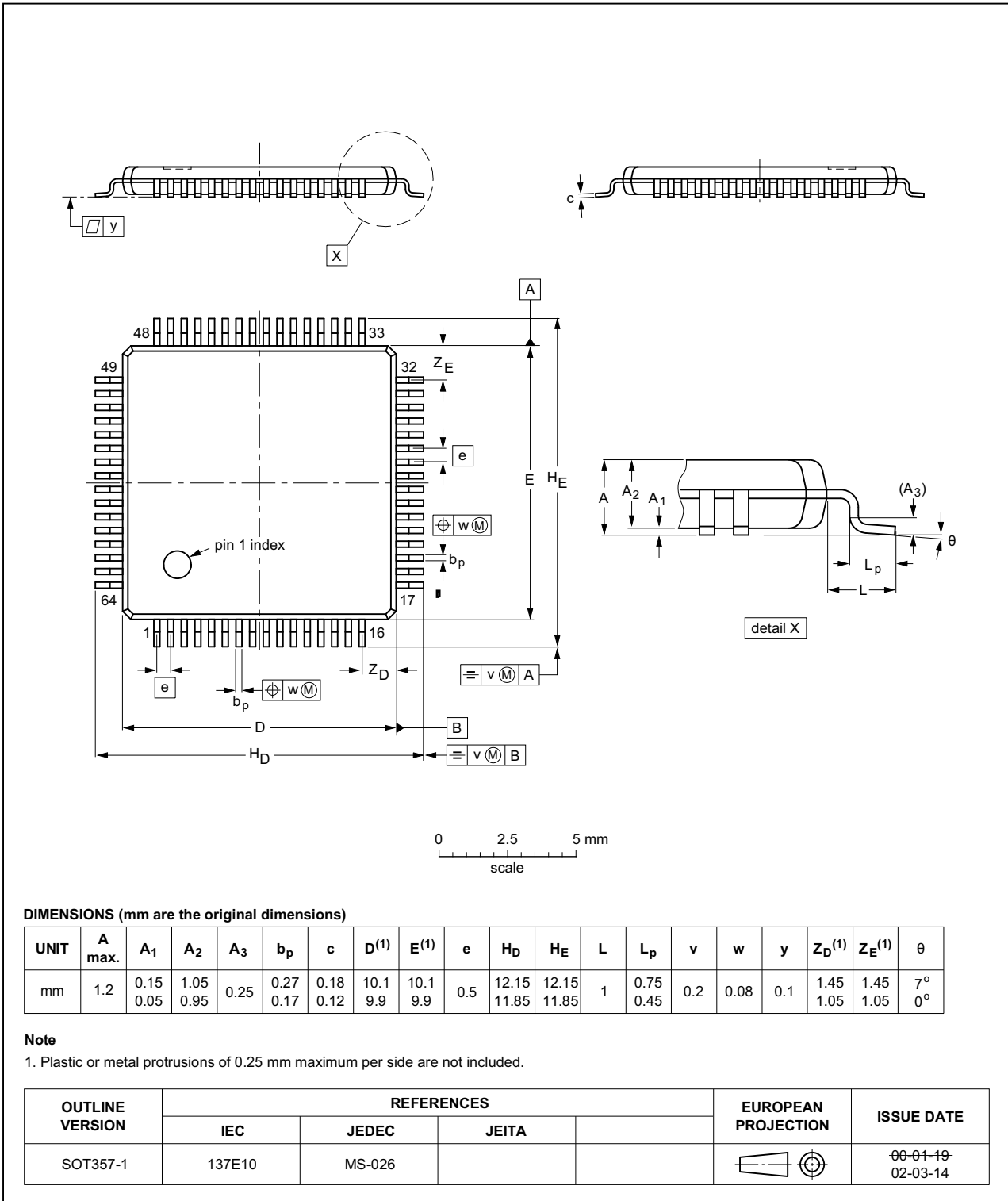


Fig 62. Package outline SOT357-1 (TQFP64)

17. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling Metal-Oxide Semiconductor (MOS) devices ensure that all normal precautions are taken as described in *JESD625-A*, *IEC 61340-5* or equivalent standards.

18. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

18.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

18.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

18.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

18.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 63](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 41](#) and [42](#)

Table 41. SnPb eutectic process (from J-STD-020D)

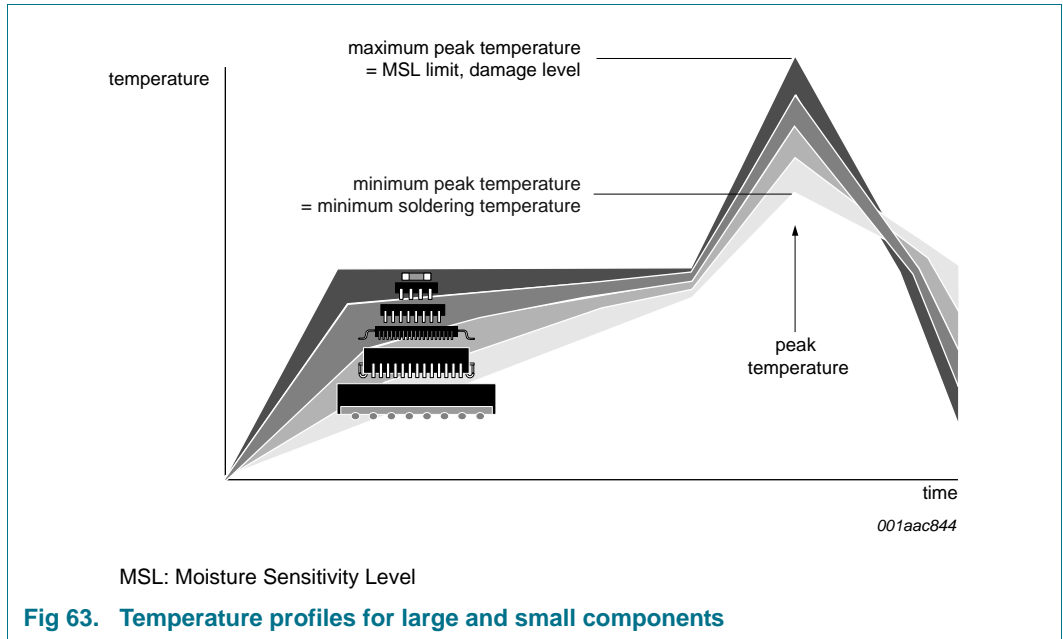
| Package thickness (mm) | Package reflow temperature (°C) | |
|------------------------|---------------------------------|-------|
| | Volume (mm ³) | |
| | < 350 | ≥ 350 |
| < 2.5 | 235 | 220 |
| ≥ 2.5 | 220 | 220 |

Table 42. Lead-free process (from J-STD-020D)

| Package thickness (mm) | Package reflow temperature (°C) | | |
|------------------------|---------------------------------|-------------|--------|
| | Volume (mm ³) | | |
| | < 350 | 350 to 2000 | > 2000 |
| < 1.6 | 260 | 260 | 260 |
| 1.6 to 2.5 | 260 | 250 | 245 |
| > 2.5 | 250 | 245 | 245 |

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 63](#).



For further information on temperature profiles, refer to Application Note AN10365 “Surface mount reflow soldering description”.

19. Appendix

19.1 LCD segment driver selection

Table 43. Selection of LCD segment drivers

| Type name | Number of elements at MUX | | | | | | | V _{DD} (V) | V _{LCD} (V) | f _{fr} (Hz) | V _{LCD} (V) charge pump | V _{LCD} (V) temperature compensat. | T _{amb} (°C) | Interface | Package | AEC- Q100 |
|------------|---------------------------|-----|-----|-----|-----|-----|-----|---------------------|----------------------|--------------------------|--|---|-----------------------|------------------------|----------|--------------|
| | 1:1 | 1:2 | 1:3 | 1:4 | 1:6 | 1:8 | 1:9 | | | | | | | | | |
| PCA8553DTT | 40 | 80 | 120 | 160 | - | - | - | 1.8 to 5.5 | 1.8 to 5.5 | 32 to 256 ^[1] | N | N | -40 to 105 | I ² C / SPI | TSSOP56 | Y |
| PCA8546ATT | - | - | - | 176 | - | - | - | 1.8 to 5.5 | 2.5 to 9 | 60 to 300 ^[1] | N | N | -40 to 95 | I ² C | TSSOP56 | Y |
| PCA8546BTT | - | - | - | 176 | - | - | - | 1.8 to 5.5 | 2.5 to 9 | 60 to 300 ^[1] | N | N | -40 to 95 | SPI | TSSOP56 | Y |
| PCA8547AHT | 44 | 88 | - | 176 | - | - | - | 1.8 to 5.5 | 2.5 to 9 | 60 to 300 ^[1] | Y | Y | -40 to 95 | I ² C | TQFP64 | Y |
| PCA8547BHT | 44 | 88 | - | 176 | - | - | - | 1.8 to 5.5 | 2.5 to 9 | 60 to 300 ^[1] | Y | Y | -40 to 95 | SPI | TQFP64 | Y |
| PCF85134HL | 60 | 120 | 180 | 240 | - | - | - | 1.8 to 5.5 | 2.5 to 6.5 | 82 | N | N | -40 to 85 | I ² C | LQFP80 | N |
| PCA85134H | 60 | 120 | 180 | 240 | - | - | - | 1.8 to 5.5 | 2.5 to 8 | 82 | N | N | -40 to 95 | I ² C | LQFP80 | Y |
| PCA8543AHL | 60 | 120 | - | 240 | - | - | - | 2.5 to 5.5 | 2.5 to 9 | 60 to 300 ^[1] | Y | Y | -40 to 105 | I ² C | LQFP80 | Y |
| PCF8545ATT | - | - | - | 176 | 252 | 320 | - | 1.8 to 5.5 | 2.5 to 5.5 | 60 to 300 ^[1] | N | N | -40 to 85 | I ² C | TSSOP56 | N |
| PCF8545BTT | - | - | - | 176 | 252 | 320 | - | 1.8 to 5.5 | 2.5 to 5.5 | 60 to 300 ^[1] | N | N | -40 to 85 | SPI | TSSOP56 | N |
| PCF8536AT | - | - | - | 176 | 252 | 320 | - | 1.8 to 5.5 | 2.5 to 9 | 60 to 300 ^[1] | N | N | -40 to 85 | I ² C | TSSOP56 | N |
| PCF8536BT | - | - | - | 176 | 252 | 320 | - | 1.8 to 5.5 | 2.5 to 9 | 60 to 300 ^[1] | N | N | -40 to 85 | SPI | TSSOP56 | N |
| PCA8536AT | - | - | - | 176 | 252 | 320 | - | 1.8 to 5.5 | 2.5 to 9 | 60 to 300 ^[1] | N | N | -40 to 95 | I ² C | TSSOP56 | Y |
| PCA8536BT | - | - | - | 176 | 252 | 320 | - | 1.8 to 5.5 | 2.5 to 9 | 60 to 300 ^[1] | N | N | -40 to 95 | SPI | TSSOP56 | Y |
| PCF8537AH | 44 | 88 | - | 176 | 276 | 352 | - | 1.8 to 5.5 | 2.5 to 9 | 60 to 300 ^[1] | Y | Y | -40 to 85 | I ² C | TQFP64 | N |
| PCF8537BH | 44 | 88 | - | 176 | 276 | 352 | - | 1.8 to 5.5 | 2.5 to 9 | 60 to 300 ^[1] | Y | Y | -40 to 85 | SPI | TQFP64 | N |
| PCA8537AH | 44 | 88 | - | 176 | 276 | 352 | - | 1.8 to 5.5 | 2.5 to 9 | 60 to 300 ^[1] | Y | Y | -40 to 95 | I ² C | TQFP64 | Y |
| PCA8537BH | 44 | 88 | - | 176 | 276 | 352 | - | 1.8 to 5.5 | 2.5 to 9 | 60 to 300 ^[1] | Y | Y | -40 to 95 | SPI | TQFP64 | Y |
| PCA9620H | 60 | 120 | - | 240 | 320 | 480 | - | 2.5 to 5.5 | 2.5 to 9 | 60 to 300 ^[1] | Y | Y | -40 to 105 | I ² C | LQFP80 | Y |
| PCA9620U | 60 | 120 | - | 240 | 320 | 480 | - | 2.5 to 5.5 | 2.5 to 9 | 60 to 300 ^[1] | Y | Y | -40 to 105 | I ² C | Bare die | Y |
| PCF8576DU | 40 | 80 | 120 | 160 | - | - | - | 1.8 to 5.5 | 2.5 to 6.5 | 77 | N | N | -40 to 85 | I ² C | Bare die | N |
| PCF8576EUG | 40 | 80 | 120 | 160 | - | - | - | 1.8 to 5.5 | 2.5 to 6.5 | 77 | N | N | -40 to 85 | I ² C | Bare die | N |
| PCA8576FUG | 40 | 80 | 120 | 160 | - | - | - | 1.8 to 5.5 | 2.5 to 8 | 200 | N | N | -40 to 105 | I ² C | Bare die | Y |
| PCF85133U | 80 | 160 | 240 | 320 | - | - | - | 1.8 to 5.5 | 2.5 to 6.5 | 82, 110 ^[2] | N | N | -40 to 85 | I ² C | Bare die | N |
| PCA85133U | 80 | 160 | 240 | 320 | - | - | - | 1.8 to 5.5 | 2.5 to 8 | 82, 110 ^[2] | N | N | -40 to 95 | I ² C | Bare die | Y |

Table 43. Selection of LCD segment drivers ...continued

| Type name | Number of elements at MUX | | | | | | | V _{DD} (V) | V _{LCD} (V) | f _{fr} (Hz) | V _{LCD} (V) charge pump | V _{LCD} (V) temperature compensat. | T _{amb} (°C) | Interface | Package | AEC- Q100 |
|------------|---------------------------|-----|-----|-----|-----|-----|-----|---------------------|----------------------|---------------------------|--|---|-----------------------|------------------------|----------|--------------|
| | 1:1 | 1:2 | 1:3 | 1:4 | 1:6 | 1:8 | 1:9 | | | | | | | | | |
| PCA85233UG | 80 | 160 | 240 | 320 | - | - | - | 1.8 to 5.5 | 2.5 to 8 | 150, 220 ^[2] | N | N | -40 to 105 | I ² C | Bare die | Y |
| PCF85132U | 160 | 320 | 480 | 640 | - | - | - | 1.8 to 5.5 | 1.8 to 8 | 60 to 90 ^[1] | N | N | -40 to 85 | I ² C | Bare die | N |
| PCA8530DUG | 102 | 204 | - | 408 | - | - | - | 2.5 to 5.5 | 4 to 12 | 45 to 300 ^[1] | Y | Y | -40 to 105 | I ² C / SPI | Bare die | Y |
| PCA85132U | 160 | 320 | 480 | 640 | - | - | - | 1.8 to 5.5 | 1.8 to 8 | 60 to 90 ^[1] | N | N | -40 to 95 | I ² C | Bare die | Y |
| PCA85232U | 160 | 320 | 480 | 640 | - | - | - | 1.8 to 5.5 | 1.8 to 8 | 117 to 176 ^[1] | N | N | -40 to 95 | I ² C | Bare die | Y |
| PCF8538UG | 102 | 204 | - | 408 | 612 | 816 | 918 | 2.5 to 5.5 | 4 to 12 | 45 to 300 ^[1] | Y | Y | -40 to 85 | I ² C / SPI | Bare die | N |
| PCA8538UG | 102 | 204 | - | 408 | 612 | 816 | 918 | 2.5 to 5.5 | 4 to 12 | 45 to 300 ^[1] | Y | Y | -40 to 105 | I ² C / SPI | Bare die | Y |

[1] Software programmable.

[2] Hardware selectable.

20. Abbreviations

Table 44. Abbreviations

| Acronym | Description |
|------------------|---|
| AEC | Automotive Electronics Council |
| CMOS | Complementary Metal Oxide Semiconductor |
| DC | Direct Current |
| EPROM | Erasable Programmable Read-Only Memory |
| HBM | Human Body Model |
| I ² C | Inter-Integrated Circuit bus |
| IC | Integrated Circuit |
| LCD | Liquid Crystal Display |
| LSB | Least Significant Bit |
| MSB | Most Significant Bit |
| MSL | Moisture Sensitivity Level |
| MUX | Multiplexer |
| OTP | One Time Programmable |
| PCB | Printed-Circuit Board |
| POR | Power-On Reset |
| RC | Resistance-Capacitance |
| RAM | Random Access Memory |
| RMS | Root Mean Square |
| SCL | Serial Clock Line |
| SDA | Serial DATA line |
| SMD | Surface Mount Device |
| SPI | Serial Peripheral Interface |

21. References

- [1] **AN10365** — Surface mount reflow soldering description
- [2] **AN10853** — ESD and EMC sensitivity of IC
- [3] **IEC 60134** — Rating systems for electronic tubes and valves and analogous semiconductor devices
- [4] **IEC 61340-5** — Protection of electronic devices from electrostatic phenomena
- [5] **IPC/JEDEC J-STD-020D** — Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices
- [6] **JESD22-A114** — Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)
- [7] **JESD22-C101** — Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components
- [8] **JESD78** — IC Latch-Up Test
- [9] **JESD625-A** — Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices
- [10] **NX3-00092** — NXP store and transport requirements
- [11] **SNV-FA-01-02** — Marking Formats Integrated Circuits
- [12] **UM10204** — I²C-bus specification and user manual

22. Revision history

Table 45. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|----------------|---|--------------------|---------------|-------------|
| PCA8537 v.2 | 20150407 | Product data sheet | - | PCA8537 v.1 |
| Modifications: | <ul style="list-style-type: none">• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.• Legal texts have been adapted to the new company name where appropriate.• Adjusted Figure 32• Fixed typos | | | |
| PCA8537 v.1 | 20120531 | Product data sheet | - | - |

23. Legal information

23.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

23.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

23.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use in automotive applications — This NXP Semiconductors product has been qualified for use in automotive applications. Unless otherwise agreed in writing, the product is not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

23.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

I²C-bus — logo is a trademark of NXP Semiconductors N.V.

24. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

25. Tables

| | | | |
|---|----|---|----|
| Table 1. Ordering information | 2 | Table 40. Timing characteristics: SPI-bus | 66 |
| Table 2. Ordering options | 2 | Table 41. SnPb eutectic process (from J-STD-020D) | 70 |
| Table 3. Marking codes | 2 | Table 42. Lead-free process (from J-STD-020D) | 70 |
| Table 4. Pin description of PCA8537AH and PCA8537BH | 6 | Table 43. Selection of LCD segment drivers | 72 |
| Table 5. Commands of PCA8537 | 7 | Table 44. Abbreviations | 74 |
| Table 6. Initialize - initialize command bit description | 8 | Table 45. Revision history | 76 |
| Table 7. OTP-refresh - OTP-refresh command bit description | 8 | | |
| Table 8. Oscillator-ctrl - oscillator control command bit description | 8 | | |
| Table 9. Charge-pump-ctrl - charge pump control command bit description | 9 | | |
| Table 10. Temp-msr-ctrl - temperature measurement control command bit description | 10 | | |
| Table 11. Temp-comp - temperature compensation coefficients command | 10 | | |
| Table 12. Set-VPR - set VPR command bit description | 11 | | |
| Table 13. Display-enable - display enable command bit description | 11 | | |
| Table 14. Set-MUX-mode - set multiplex drive mode command bit description | 12 | | |
| Table 15. Set-bias-mode - set bias mode command bit description | 12 | | |
| Table 16. Load-data-pointer - load data pointer command bit description | 12 | | |
| Table 17. Frame frequency - frame frequency and output clock frequency command bit description | 13 | | |
| Table 18. Frame frequency values | 13 | | |
| Table 19. Bank-select - bank select command bit description | 14 | | |
| Table 20. Write-RAM-data - write RAM data command bit description | 14 | | |
| Table 21. Temp-read - temperature readout command bit description | 15 | | |
| Table 22. Invmode_ctrl - drive scheme inversion command bit description | 15 | | |
| Table 23. Temp-filter - digital temperature filter command bit description | 16 | | |
| Table 24. Reset state | 17 | | |
| Table 25. Selection of display configurations | 23 | | |
| Table 26. Temperature measurement update rate | 28 | | |
| Table 27. Temperature coefficients | 30 | | |
| Table 28. Calculation of the V_{LCD} offset voltage | 31 | | |
| Table 29. LCD drive modes: summary of characteristics | 32 | | |
| Table 30. Mapping of output pins and corresponding signals with respect to driving mode | 42 | | |
| Table 31. Control byte description | 50 | | |
| Table 32. I ² C slave address byte | 53 | | |
| Table 33. R/W bit description | 53 | | |
| Table 34. Serial interface | 55 | | |
| Table 35. Subaddress byte definition | 55 | | |
| Table 36. Limiting values | 59 | | |
| Table 37. Static characteristics | 60 | | |
| Table 38. Dynamic characteristics | 64 | | |
| Table 39. Timing characteristics: I ² C-bus | 65 | | |

26. Figures

| | | | | | |
|---------|---|----|---------|--|----|
| Fig 1. | Block diagram of PCA8537AH. | 3 | Fig 26. | Waveforms for the 1:2 multiplex drive mode with $\frac{1}{3}$ bias (line inversion mode) | 36 |
| Fig 2. | Block diagram of PCA8537BH. | 4 | Fig 27. | Waveforms for the 1:4 multiplex drive mode with $\frac{1}{3}$ bias (line inversion mode) | 37 |
| Fig 3. | Pin configuration for TQFP64 (PCA8537AH). | 5 | Fig 28. | Waveforms for 1:6 multiplex drive mode with $\frac{1}{3}$ bias (line inversion mode) | 38 |
| Fig 4. | Pin configuration for TQFP64 (PCA8537BH). | 5 | Fig 29. | Waveforms for 1:6 multiplex drive mode with $\frac{1}{4}$ bias (line inversion mode) | 39 |
| Fig 5. | Recommended start-up sequence when using the internal charge pump and the internal clock signal | 18 | Fig 30. | Waveforms for 1:8 multiplex drive mode with $\frac{1}{4}$ bias (line inversion mode) | 40 |
| Fig 6. | Recommended start-up sequence when using an external supplied V_{LCD} and the internal clock signal | 19 | Fig 31. | Waveforms for 1:8 multiplex drive mode with $\frac{1}{4}$ bias (frame inversion mode) | 41 |
| Fig 7. | Recommended start-up sequence when using the internal charge pump and an external clock signal | 19 | Fig 32. | Display RAM bitmap | 44 |
| Fig 8. | Recommended start-up sequence when using an external supplied V_{LCD} and an external clock signal | 20 | Fig 33. | Display RAM filling order in static drive mode | 46 |
| Fig 9. | Recommended power-down sequence for minimum power-down current when using the internal charge pump and the internal clock signal | 20 | Fig 34. | Discarded bits at the end of data transmission | 46 |
| Fig 10. | Recommended power-down sequence when using an external supplied V_{LCD} and the internal clock signal | 21 | Fig 35. | Display RAM filling order in 1:2 multiplex drive mode | 46 |
| Fig 11. | Recommended power-down sequence when using the internal charge pump and an external clock signal | 21 | Fig 36. | Display RAM filling order in 1:4 multiplex drive mode | 47 |
| Fig 12. | Recommended power-down sequence for minimum power-down current when using an external supplied V_{LCD} and an external clock signal | 22 | Fig 37. | Display RAM filling order in 1:6 multiplex drive mode | 48 |
| Fig 13. | Example of displays suitable for PCA8537 | 23 | Fig 38. | Display RAM filling order in 1:8 multiplex drive mode | 48 |
| Fig 14. | Typical I ² C system configuration when using the internal V_{LCD} generation | 23 | Fig 39. | Bank selection. | 49 |
| Fig 15. | Typical SPI system configuration when using an external V_{LCD} | 24 | Fig 40. | Example of the Bank-select command with multiplex drive mode 1:4 | 49 |
| Fig 16. | V_{LCD} generation including temperature compensation | 25 | Fig 41. | Control byte format | 50 |
| Fig 17. | V_{LCD} programming of PCA8537 (assuming $VT[7:0] = 0h$) | 26 | Fig 42. | Bit transfer. | 51 |
| Fig 18. | Charge pump driving capability with $V_{DD2} = 3.3 V$ | 27 | Fig 43. | Definition of START and STOP conditions | 51 |
| Fig 19. | Charge pump driving capability with $V_{DD2} = 5.0 V$ | 28 | Fig 44. | System configuration. | 52 |
| Fig 20. | Temperature measurement block with digital temperature filter | 29 | Fig 45. | Acknowledgement on the I ² C-bus. | 52 |
| Fig 21. | Temperature measurement delay during ramping up-down of the environment temperature | 29 | Fig 46. | I ² C-bus protocol, write mode. | 54 |
| Fig 22. | Example of segmented temperature coefficients | 30 | Fig 47. | I ² C-bus protocol, read mode. | 54 |
| Fig 23. | Electro-optical characteristic: relative transmission curve of the liquid | 33 | Fig 48. | Data transfer overview | 55 |
| Fig 24. | Static drive mode waveforms (line inversion mode). | 34 | Fig 49. | SPI-bus write example | 56 |
| Fig 25. | Waveforms for the 1:2 multiplex drive mode with $\frac{1}{2}$ bias (line inversion mode) | 35 | Fig 50. | SPI-bus write example | 56 |
| | | | Fig 51. | SPI-bus read example. | 57 |
| | | | Fig 52. | Device protection diagram for PCA8537AH | 58 |
| | | | Fig 53. | Device protection diagram for PCA8537BH | 58 |
| | | | Fig 54. | LCD voltage variation with respect to temperature. | 62 |
| | | | Fig 55. | Typical I_{DD1} with respect to temperature | 63 |
| | | | Fig 56. | Typical I_{DD2} with respect to temperature | 63 |
| | | | Fig 57. | Typical $I_{DD(LCD)}$ with respect to temperature | 64 |
| | | | Fig 58. | Driver timing waveforms | 64 |
| | | | Fig 59. | RESET timing | 65 |
| | | | Fig 60. | I ² C-bus timing waveforms | 66 |
| | | | Fig 61. | SPI-bus timing. | 67 |
| | | | Fig 62. | Package outline SOT357-1 (TQFP64) | 68 |
| | | | Fig 63. | Temperature profiles for large and small components. | 71 |

27. Contents

| | | | | | |
|------------|--|-----------|----------------|---|-----------|
| 1 | General description | 1 | 8.4.4 | Temperature measurement and temperature compensation of V_{LCD} | 28 |
| 2 | Features and benefits | 1 | 8.4.4.1 | Temperature readout | 28 |
| 3 | Applications | 2 | 8.4.4.2 | Temperature adjustment of the V_{LCD} | 30 |
| 4 | Ordering information | 2 | 8.4.5 | LCD voltage selector | 31 |
| 4.1 | Ordering options | 2 | 8.4.5.1 | Electro-optical performance | 33 |
| 5 | Marking | 2 | 8.4.6 | LCD drive mode waveforms | 34 |
| 6 | Block diagram | 3 | 8.4.6.1 | Static drive mode | 34 |
| 7 | Pinning information | 5 | 8.4.6.2 | 1:2 multiplex drive mode | 35 |
| 7.1 | Pinning | 5 | 8.4.6.3 | 1:4 multiplex drive mode | 37 |
| 7.2 | Pin description | 6 | 8.4.6.4 | 1:6 multiplex drive mode | 38 |
| 8 | Functional description | 7 | 8.4.6.5 | 1:8 multiplex drive mode | 40 |
| 8.1 | Commands of PCA8537 | 7 | 8.5 | Backplane and segment outputs | 42 |
| 8.1.1 | Command: Initialize | 7 | 8.5.1 | Backplane outputs | 42 |
| 8.1.2 | Command: OTP-refresh | 8 | 8.5.1.1 | 1:8 multiplex drive mode | 42 |
| 8.1.3 | Command: Oscillator-ctrl | 8 | 8.5.1.2 | 1:6 multiplex drive mode | 42 |
| 8.1.3.1 | Oscillator | 8 | 8.5.1.3 | 1:4 multiplex drive mode | 42 |
| 8.1.3.2 | Internal oscillator | 8 | 8.5.1.4 | 1:2 multiplex drive mode | 42 |
| 8.1.3.3 | External clock | 9 | 8.5.1.5 | Static drive mode | 43 |
| 8.1.4 | Command: Charge-pump-ctrl | 9 | 8.5.2 | Segment outputs | 43 |
| 8.1.5 | Command: Temp-msr-ctrl | 10 | 8.5.2.1 | Static, 1:8, 1:4, 1:2 multiplex drive mode | 43 |
| 8.1.6 | Command: Temp-comp | 10 | 8.5.2.2 | 1:6 multiplex drive mode | 43 |
| 8.1.7 | Command: Set-VPR | 11 | 8.6 | Display controller | 43 |
| 8.1.8 | Command: Display-enable | 11 | 8.7 | Display register | 43 |
| 8.1.9 | Command: Set-MUX-mode | 12 | 8.8 | Display RAM | 43 |
| 8.1.10 | Command: Set-bias-mode | 12 | 8.8.1 | Data pointer | 45 |
| 8.1.11 | Command: Load-data-pointer | 12 | 8.8.2 | RAM filling in static drive mode | 45 |
| 8.1.12 | Command: Frame-frequency | 13 | 8.8.3 | RAM filling in 1:2 multiplex drive mode | 46 |
| 8.1.12.1 | Timing and frame frequency | 14 | 8.8.4 | RAM filling in 1:4 multiplex drive mode | 47 |
| 8.1.13 | Command: Bank-select | 14 | 8.8.5 | RAM filling in 1:6 multiplex drive mode | 47 |
| 8.1.14 | Command: Write-RAM-data | 14 | 8.8.6 | RAM filling in 1:8 multiplex drive mode | 48 |
| 8.1.15 | Command: Temp-read | 15 | 8.9 | Bank selection | 49 |
| 8.1.16 | Command: Invmode_ctrl | 15 | 8.9.1 | Input bank selection | 49 |
| 8.1.17 | Command: Temp-filter | 16 | 8.9.2 | Output bank selection | 50 |
| 8.2 | Start-up and shut-down | 16 | 9 | Bus interfaces | 50 |
| 8.2.1 | Power-On Reset (POR) | 16 | 9.1 | Control byte | 50 |
| 8.2.2 | RESET pin function | 17 | 9.2 | I ² C-bus interface characteristics (PCA8537AH) | 51 |
| 8.2.3 | Recommended start-up sequences | 17 | 9.2.1 | Bit transfer | 51 |
| 8.2.4 | Recommended sequences to enter power-down mode | 20 | 9.2.2 | START and STOP conditions | 51 |
| 8.3 | Possible display configurations | 22 | 9.2.3 | System configuration | 51 |
| 8.4 | LCD supply voltage | 24 | 9.2.4 | Acknowledge | 52 |
| 8.4.1 | External V_{LCD} supply | 24 | 9.2.5 | I ² C-bus controller | 52 |
| 8.4.2 | Internal V_{LCD} generation | 24 | 9.2.6 | Input filters | 53 |
| 8.4.3 | Charge pump | 26 | 9.2.7 | I ² C-bus slave address | 53 |
| 8.4.3.1 | Charge pump configuration | 26 | 9.2.8 | I ² C-bus protocol | 53 |
| 8.4.3.2 | Charge pump driving capability | 26 | 9.2.9 | Data read | 54 |
| | | | 9.3 | SPI-bus interface (PCA8537BH) | 55 |

continued >>

| | | |
|-----------|--|-----------|
| 9.3.1 | Data transmission | 55 |
| 9.3.2 | Data read | 56 |
| 10 | Internal circuitry | 58 |
| 11 | Safety notes | 58 |
| 12 | Limiting values | 59 |
| 13 | Static characteristics | 60 |
| 14 | Dynamic characteristics | 64 |
| 15 | Test information | 67 |
| 15.1 | Quality information | 67 |
| 16 | Package outline | 68 |
| 17 | Handling information | 69 |
| 18 | Soldering of SMD packages | 69 |
| 18.1 | Introduction to soldering | 69 |
| 18.2 | Wave and reflow soldering | 69 |
| 18.3 | Wave soldering | 70 |
| 18.4 | Reflow soldering | 70 |
| 19 | Appendix | 72 |
| 19.1 | LCD segment driver selection | 72 |
| 20 | Abbreviations | 74 |
| 21 | References | 75 |
| 22 | Revision history | 76 |
| 23 | Legal information | 77 |
| 23.1 | Data sheet status | 77 |
| 23.2 | Definitions | 77 |
| 23.3 | Disclaimers | 77 |
| 23.4 | Trademarks | 78 |
| 24 | Contact information | 78 |
| 25 | Tables | 79 |
| 26 | Figures | 80 |
| 27 | Contents | 81 |

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP Semiconductors N.V. 2015.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 7 April 2015

Document identifier: PCA8537